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HIP2103, HIP2104 Evaluation Board User's Guide

Introduction

The HIP2103_4MBEVAL1Z is an evaluation tool for the HIP2103 and HIP2104 half bridge MOSFET drivers. This tool consists of a mother board and HIP2103DBEVAL1Z and HIP2104DBEVAL1Z evaluation daughter cards. The mother board platform provides an on-board microcontroller that is used to generate appropriate control inputs to the HIP2103 or HIP2104. The frequency, the PWM duty cycle, and the dead-time provided by the microcontroller are user adjustable.

For customers who desire to provide their own external signals, the on-board controller can be configured to allow the daughter cards to be controlled by externally provided inputs.

The daughter cards can also be used as stand-alone units mounted on a customer designed main board that incorporates customer selected bridge FETs and any other external circuits desired. The daughter cards have optional circuits so that the HIP2103 or HIP2104 can be configured as required by the customer's application.

Specifications

Bridge Bias Voltage (V_{BAT})	5V minimum, 50V maximum operating **including** transients
External Bias for Microcontroller	3.3V - 5.0V, ~30mA
Maximum Bridge Current	20A
PWM Switching Frequency	5kHz to 40kHz in 5kHz increments
PWM Duty Cycle	adjustable from 0% to ~ 98%
Dead-time	0.0µs to 2.8µs in 400ns increments
Large Terminal Blocks	15A each connection
Small Terminal Blocks	6A each connection

Scope

This application note covers the use of the HIP2103_4 mother board and the HIP2103_4 daughter cards. Details for setting up and using the microcontroller are covered. Assembly options on the motherboard are also reviewed. Sample waveforms are also provided.

The microcontroller firmware is provided on request but the only support offered by Intersil will be for bug corrections. Please refer to Microchip for details on the use of the PIC18F2431.

Physical Layout

The HIP2103_4MBEVAL1Z board is 84mm by 94mm. The tallest component is the RJ25 connector. The total height is 38mm. Multiple inputs have miniature terminal blocks and the high current battery inputs and load outputs have larger terminal blocks rated for 15A each connection. Three push-buttons are used for RESET, START/STOP, and SLEEP functions. An on-board potentiometer is used to adjust the duty cycle.

The 6 position DIP switch is used to setup the PWM switching frequency (positions 1, 2, and 3) and the dead-time (positions 4, 5, and 6). One specific combination of DIP switch settings (all positions set to on) disables the signals from the microcontroller and enables all of the external inputs.

For those customers who would like to modify the firmware of the PIC18F2431 microcontroller, an RJ25 connector is provided for easy connection with Microchip firmware development tools (not provided or supported by Intersil).

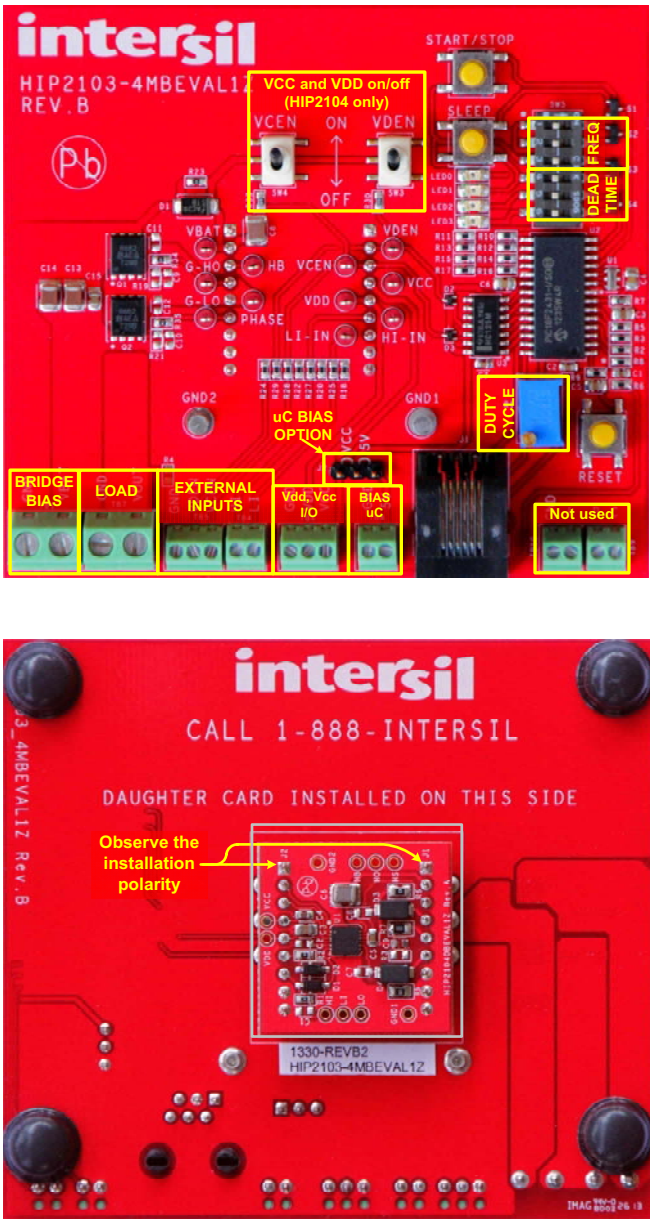


FIGURE 1. HIP2103_4MBEVAL1Z, FRONT AND BACK VIEWS

Block Diagram

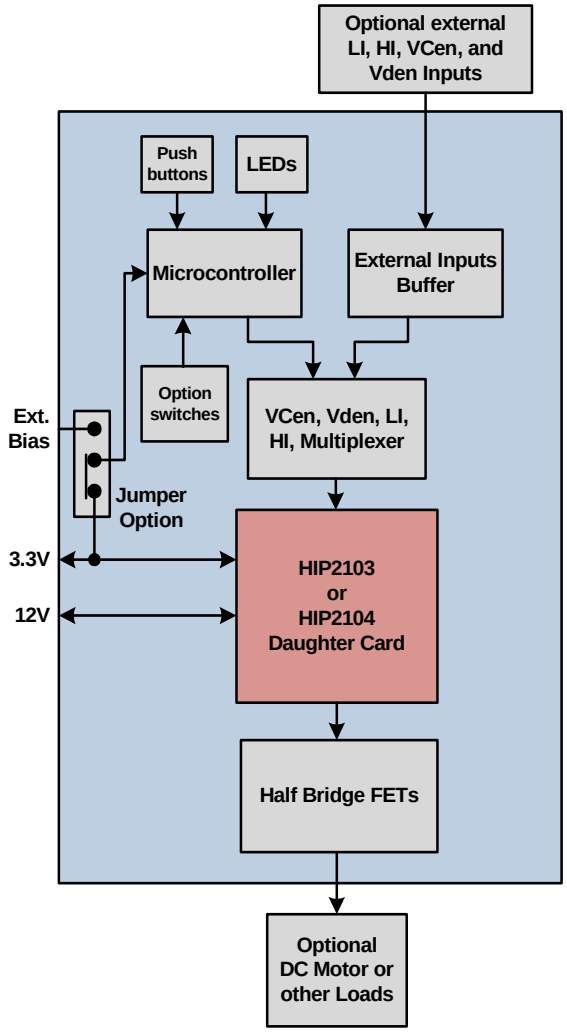


FIGURE 2. HIP2103_4MBEVAL1Z, BLOCK DIAGRAM

The HIP2103_4 evaluation board is a fully self contained test platform to evaluation the HIP2103 or the HIP2104 which are provided on daughter cards.

Evaluation Board Application

The HIP2103_4MBEVAL1Z mother board and associated daughter cards are the same test boards as used by the Intersil application engineers and I.C. designers to evaluate the performance of the HIP2103 and HIP2104 MOSFET drivers.

Bias Supplies

The HIP2103_4MBEVAL1Z mother board requires a current limited lab supply (0V to 50V) for the VBAT and GND inputs on TB1. The current capacity is dependant on the users desired load if any.

An external 3.3V to 5V bias supply (~25mA) is required for the microcontroller and associated circuits. Alternatively, the VCC output of the HIP2104 daughter card can be used to provide the 3.3V bias for the microcontroller as intended in a real application. The jumper strap option, J2, is used to select the appropriate bias source labeled VCC from the HIP2104 or 5V from an external bias connected to 5V and GND on TB8.

The 12V bias for the HIP2103 daughter card must be supplied by an external source connected to VDD and GND of TB6.

An external 12V bias is not required for the HIP2104 daughter card because VDD is provided internally by the HIP2104 driver.

MicroController and Associated Circuits

The PWM frequency and the dead-time options of the microcontroller are configured by the SW5 DIP switch. Refer to the chart on the mother board schematic (page 9) for the DIP switch settings or to Table 1. The DIP switch settings are read only once after the Start/Stop button is pressed to start the PWM. Any changes to the frequency or dead-time settings are not recognized until the PWM is stopped then re-started.

Turning the potentiometer, R1, fully counter clockwise (CCW) reduces the duty cycle of the output of the bridge to a minimum. Turning fully clockwise results with a maximum duty cycle. The duty cycle is proportional to the tap voltage of the potentiometer independent of the PWM frequency. The dead-time subtracts from the duty cycle period on the leading edge of the HI and LI inputs to the daughter cards altering the actual duty cycle.

To emulate controllers that may to be used by customers that do not have the ability to generate dead-time, the dead-time of the microcontroller can be set to zero. On the daughter cards, an optional RCD circuit is provided for the LI and HI inputs of the HIP2103, HIP2104 to generate dead-time.

Be cautious if the zero dead-time option is selected when the HIP2103, HIP2104 daughter cards are not configured for delays with the RCD circuit as this will result with shoot-thru currents in the bridge.

Four LEDs are used to indicate the operating status of the microcontroller. Refer to the Setup and Operating Instructions section for complete details.

Half Bridge

The bridge is composed of two (SiR662DP) 60A, 60V, MOSFETs. Each FET has an optional gate to source and drain to gate capacitors to allow the emulation of FETs with larger capacitances if desired. An optional series gate resistor is also provided for each bridge FET that can also be used the emulate the internal gate resistance. The current rating of these SiR662DP MOSFETs was chosen primarily to eliminate the need of a heat sink when operating with heavy current loads. The maximum output load current is constrained by the current rating of the VBAT (TB1) and the Vout (TB7) terminal blocks. If a load current higher than 15A is desired, it is recommended that the battery and load wires are soldered directly to the solder pads of the TB1 and TB2 terminal blocks on the bottom of the PCB.

The bridge bias source is connected to the GND_VBAT terminal block (TB1). The voltage source can be either a current limited power supply (recommended for initial setup) or a battery (a fuse is highly recommended).

An external load can be connected to the GND_VOUT (TB7) terminal block. The load can be of any configuration (for example

a DC motor or an LCR load) as desired by the user within the constraints of the bridge FETs and the terminal blocks.

Even though the FETs have a voltage rating of 60V, the maximum operating voltage is limited to 50V by the rating of the HS and VBAT pins on the HIP2103, HIP2104 drivers.

Daughter Cards

Two different daughter cards are provided for evaluation. These cards are mounted on the back side of the mother board to facilitate temperature testing using a temperature forcing system.

The HIP2103DBEVAL1Z and HIP2104DBEVAL1Z daughter cards are identical except for the differences between the HIP2103 and the HIP2104.

The HIP2104 has integrated LDOs for the VDD bias of the driver and VCC for the bias of the controller. VDD and VCC outputs of the HIP2104 are available on the GND_VDD_VCC terminal block (TB6). External loads on the LDOs can be connected here.

When using the HIP2103 daughter card, both VDD and VCC must come from external sources. The same terminal block used for the LDO outputs of the HIP2104 can be used as external inputs when using the HIP2103.

As mentioned previously, the J2 strap option is used to select the bias source for the microcontroller. If the 5V strap option is selected, the bias to the microcontroller will always be present (if the external source is on) even when the LDO outputs of the HIP2104 are not enabled. This is desirable during the initial setup of the evaluation board or when testing the HIP2103.

Switches and Push Buttons

The VCEN and VDEN inputs of the HIP2104, are used to enable the LDO outputs of the HIP2104. These two signals are provided by two mechanical switches, SW2 and SW3. Mechanical switches are used to demonstrate the intended use of the VCEN and VCEN inputs of the HIP2104 although digital logic signals can also be used when external inputs are optionally chosen. The debouncing feature of the VDCEN and VDEN inputs can also be observed when using the mechanical switches. Note that either of these two switches can be turned on or off randomly to demonstrate the performance of the HIP2104 when either of the LDO outputs are turned off during operation of the bridge.

Three push buttons provide control signals to the microcontroller. As usual, the reset button restarts the firmware. The Start/Stop button starts and stops the PWM signals to the LI and HI inputs of the HIP2103, HIP2104. The Sleep button turns on and off the sleep mode.

User Assembly Options

The following user optional assembly features are provided on the evaluation mother board:

- Series connected diode (D1) on the VBAT input to the HIP2104 daughter card for holding up VBAT when there is severe ripple voltage from a LI-ON battery. A zero ohm resistor (R23) shorts out this diode when not required (installed)

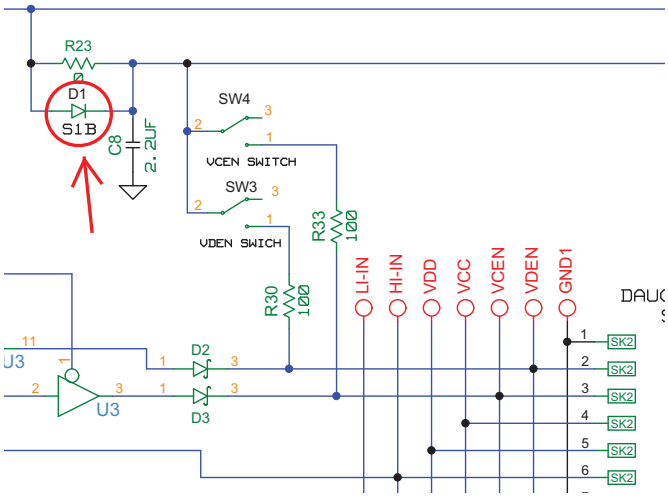


FIGURE 3. DIODE TO SUPPRESS LI-ON BATTERY RIPPLE

- Gate to source resistors on the bridge FETs. (R19 and R21 are omitted)
- Series connected gate resistors on each bridge FETs (R34 and R35 are installed with zero ohms)
- Gate to source, and gate to drain capacitor on the bridge FETs (C11, C12, C9, and C10 omitted). The capacitors can be added to emulate larger FETs.

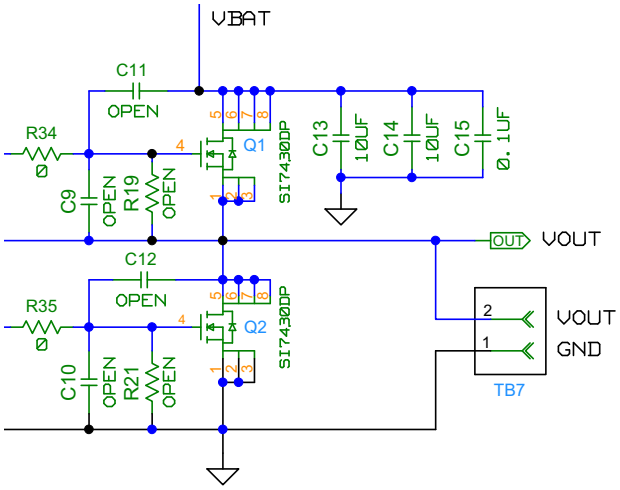


FIGURE 4. OPTIONAL RESISTORS AND CAPACITORS FOR BRIDGE FETs

The following user optional assembly features are provided on the HIP2103, HIP2104 daughter cards.

- The HO and LO outputs have options for a bypass diode across a series connected gate resistor for slower turn-on and faster turn-off of the driven bridge FET. The default configuration includes the bypass diode in parallel with a 24.9Ω resistor.

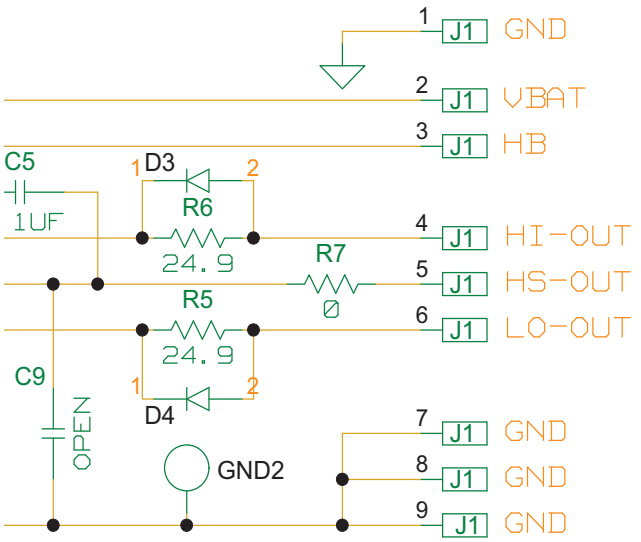


FIGURE 5. BYPASS DIODES (D3, D4) FOR SLOW TURN-ON AND FAST TURN-OFF

- The LI and HI inputs have optional RCD circuits for the purpose of generating dead-time if a controller is used that does not have built-in dead-time capability. As previously mentioned, the on-board microcontroller can be configured for no dead-time delays. The default configuration includes Schottky diodes in parallel with a zero ohm resistor.

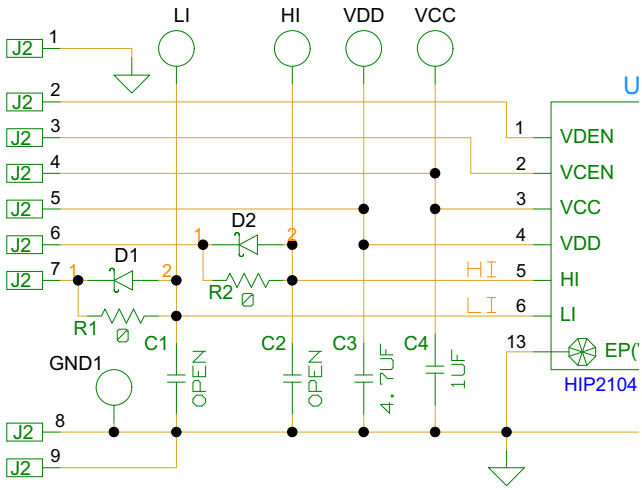


FIGURE 6. BYPASS DIODES (D1, D2) USED FOR DEAD TIME GENERATION

- The HS pin has an RC filter (R7/C7 on the HIP2103 daughter card and R7/C9 on the HIP2104 daughter card) that was required for early engineering samples (rev. A) of the HIP2103/4. This filter is not necessary for the production grade parts. The default value for R7 is zero ohms and the capacitor between HS and VSS is omitted.

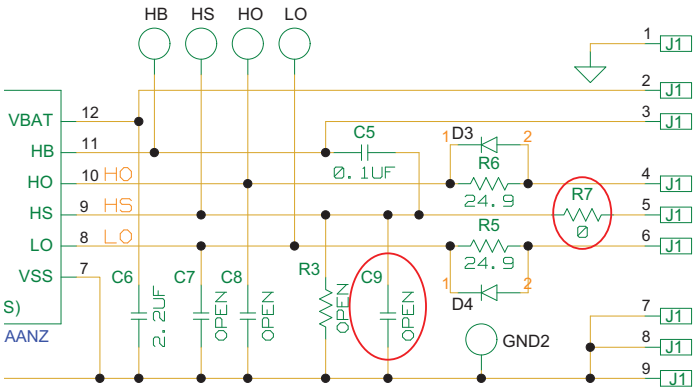


FIGURE 7. RC FILTER ON HS PIN (NOT REQUIRED)

Switching Transients

The recommended maximum operating voltage on the HS, VBAT, VCEN, and VDEN pins is 50V. This **includes** the switching transients resulting from parasitic inductance in the bridge circuit.

In the case of the VCEN and VDEN inputs, the parasitic inductance resulting from the leads to and from the mechanical switches will resonate with the input capacitance of these pins and with the paralleled external parasitic capacitance on the PCB. When operating at higher voltage levels, it is necessary to have series connected resistor, R30 and R33 (on the mother board), to dampen the ringing spike. By default, R30 and R33 are 100Ω.

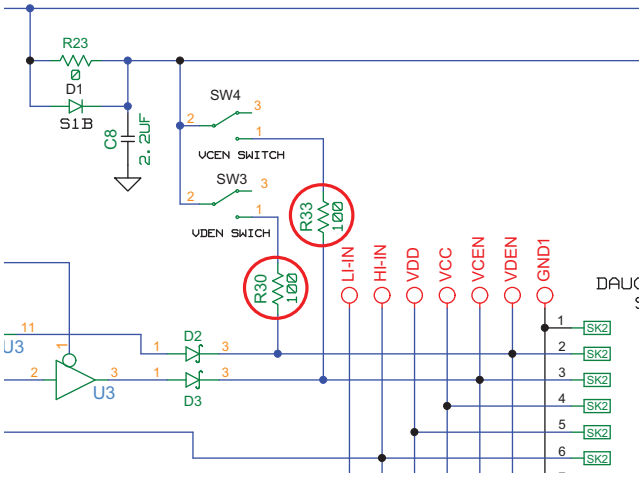


FIGURE 8. VCEN AND VDEN DAMPENING RESISTORS

A similar transient situation may occur with the HS pin. In this situation, a ringing spike can be more severe because of high speed switching from the bridge FETs, the large amplitude of switching currents, and because of parasitic inductance associated with the bridge high current PCB traces. Because the amplitude of the ringing spike also increases with the switching load current amplitude, evaluation should be over the full operating load range including fault currents. Good bridge circuit PCB design will minimize but cannot totally eliminate ringing on the HS node.

These switching transients are relatively fast. When evaluating the spikes on these pins, it is necessary to use a time base on the scope of about 100ns/division. Slower sweep speeds may mask the switching spike depending on the sample rate of the digital scope.

Other methods can also be used to reduce ringing on the HS node. Sufficiently large value gate resistors on the bridge FETs will reduce the switching speed and consequently the amplitude of the ringing. The above mentioned RC filter on the HS pin can also be used to attenuate the spike directly on the HS pin. By default, the gate resistors on the HIP2103/4 daughter cards, R5 and R6, is 24.9Ω. With this evaluation PCB layout, 24.9Ω is sufficient to prevent excessive switching transient but a customer's PCB layout may require more or less gate resistance or another method to attenuate the switching transients.

Another source of switching transients that must be dealt with is from the bridge voltage source, especially with LI-ON batteries. When the LI_ON battery load current is interrupted when the bridge turns off, the voltage from the battery can rise dramatically because of the internal inductance of the battery. The usual solution is to have sufficiently large capacitance across the bridge. This bridge bypass capacitor is effectively an LC filter working with the internal inductance of the LI-ON battery (typically a few hundred nH). If the capacitor value is large enough, the battery voltage will be close to the nominal unloaded value with minimal ripple. Another approach to reduce the amplitude of the voltage transient from the battery without increasing the size or value of the bridge capacitor is to increase the PWM switching frequency.

If it is not desirable to use relatively large value capacitors across the bridge, a clamping method must be used to limit the peak voltage ripple from the battery. In any case, a relatively small capacitor across the bridge should be used to limit the rate of change of the ripple voltage and to minimize the effects of the PCB parasitic trace inductance on the HS pin.

Another consequence of allowing a relatively large ripple voltage on the battery is that under heavy load conditions, the voltage ripple valley will drop to very low levels. Because most motor loads respond to the average voltage applied, this ripple voltage is of minimal concern. The problem is that if the valley voltage drops too low, the 12V LDO (VDD) of the HIP2104 will sag resulting with a lower gate drive voltage. The UVLO of the HIP2103/4 is 4.5V (or optionally 7.5V). If the bridge FETs are selected appropriately, this low gate drive voltage will have not significant effect except for the usual consequence of higher $r_{DS(ON)}$ of the bridge FETs.

To mitigate this problem of excessively low ripple voltage from the battery, a diode in series with the VBAT input of the HIP2104 daughter card with a capacitor to ground will hold up the voltage on VBAT (and consequently the VCC and VDD outputs) when the valley voltage is low (Figure 3). This series connected diode is an assembly option on the HIP2103_4MBEVAL1Z mother board. The default configuration has a zero ohm resistor in parallel with the diode.

Setup and Operating Instructions

The follow procedure ensures a correct setup of the evaluation board and illustrates various operating methods.

Required Lab Equipment

- Power supply (or battery), 13V minimum to 50V maximum operating for the bridge bias. The current rating of the power supply must have sufficient capacity for the external load used for testing (if any). If no load is applied, 200mA is sufficient. If a battery is the power source, it is highly recommended that an appropriate fuse be used. With a LI-ON battery, it is necessary to add sufficient capacitance (100µF or greater) across the VBAT terminal block to prevent excessive ringing.
- Bias supply, 12V at ~50mA, require for testing the HIP2103
- Bias supply, 3.3V to 5.0V at ~50mA, for testing the HIP2103
- Bench fan (only necessary when testing with large loads at elevated ambient temperatures)
- Four channel oscilloscope, ~500MHz recommended
- Current Probe (optional) when testing with external loads.
- Multimeter

Initial Configuration for the Microcontroller

The following procedure illustrates how to configure the microcontroller without applying power to the bridge.

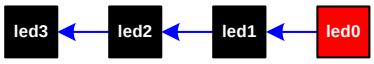
1. Connect a 5.0V bias supply to the +5V_GND terminal block (TB8). This voltage powers the microcontroller.
2. Ensure that the jumper strap on J2 is on the 5V option. This will connect the microcontroller to the external lab supply.
3. Setup the DIP switch on the mother board with the desired PWM frequency and dead-time. For the initial setup, start with 20kHz and 400ns dead-time (in bold type).

TABLE 1. DIP SWITCH OPTIONS

SWITCH POSITION	6	5	4	3	2	1	
PWM Frequency	x	x	x	0	0	0	5kHz
	x	x	x	0	0	1	10kHz
	x	x	x	0	1	0	15kHz
	x	x	x	**0**	**1**	**1**	**20kHz**
	x	x	x	1	0	0	25kHz
	x	x	x	1	0	1	30kHz
	x	x	x	1	1	0	35kHz
	x	x	x	1	1	1	40kHz
External inputs	1	1	1	1	1	1	
Dead-Time	0	0	0	x	x	x	0.000µs
	0	**0**	**1**	x	x	x	**0.400µs**
	0	1	0	x	x	x	0.800µs
	0	1	1	x	x	x	1.200µs
	1	0	0	x	x	x	1.600µs
	1	0	1	x	x	x	2.000µs
	1	1	0	x	x	x	2.400µs
	1	1	1	x	x	x	2.800µs

4. Connect scope probes on the HI and LI test points on the mother board. Set the time base to 200ns/Div. Set the vertical gain to 2V/Div. Set the trigger on the LI input at the 2.5V level with a negative edge trigger. Set the trigger position at the 400ns division (on the left side of the screen) and use the auto trigger mode.

5. Turn the duty cycle potentiometer, R1, fully counter clockwise until it clicks.
6. Turn on the lab supply. Observe that the four LEDs turn on and off, one after another. This flashing sequence indicates that power has been applied. After the initial flash, all LEDs will be off.



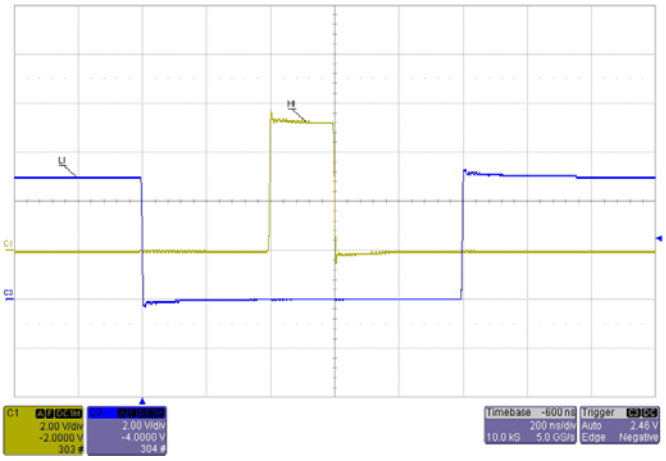
At initial turn on, leds will turn on and off one at a time starting with led0

7. Observe that the LI and HI inputs are low.
8. Press the Start/Stop push button once. The RUN LED (led0) will blink indicating that PWM signals from the controller have been enabled.

With PWM signals present on LI and HI, the RUN LED is blinking

The DIP switch options are read only when the Start/Stop button is pressed to start the PWM signals. Changing the settings while the RUN LED is flashing will have no effect. To update the DIP switch setting, change the setting, stop the PWM signals, then start again.

9. Slowly rotate the potentiometer, R1, to the right (CW) until the following waveforms appear.

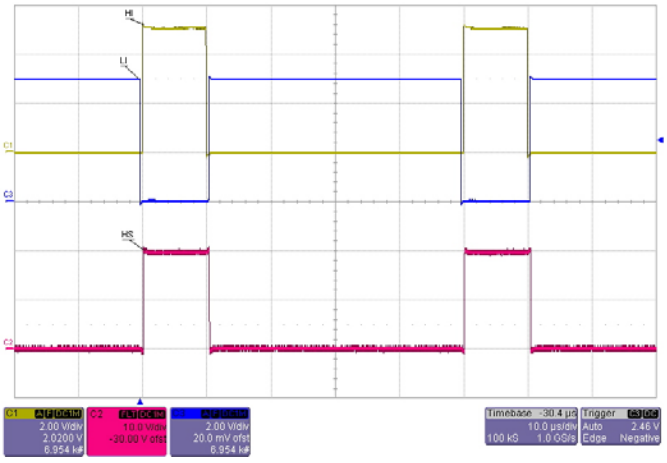


10. Confirm that a 400ns dead-time is present.
11. Rotate the potentiometer CCW to zero the PWM period.
12. Press the Start/Stop push button to disable the PWM outputs. The blinking led0 will turn off.
13. Press the Sleep button. led1 will turn on to indicate that the sleep mode is active.
14. Press the Start/Stop button. led0 will flash indicating that the PWM outputs are active. Simultaneously, led1 will turn off indicating that the sleep mode is no longer active.
15. Press the Sleep button. led0 will turn off and led1 will turn on indicating that the sleep mode is active.

Initial Setup to Evaluate the HIP2104 Daughter Card

The following procedure illustrates how to setup the daughter cards and applying power to the bridge.

1. Install a HIP2104 daughter card on the mother board. Be careful with the polarity. Incorrect installation may damage the daughter card and the mother board.
2. Connect an additional scope probe to the HS test point on the mother board. Set the vertical gain to 10V/Div and the time base to 10µs/Div.
3. Ensure that the VDEN and VCEN switches are off.
4. Connect the bridge power supply to the VBAT_GND terminal block (TB1).
5. Starting with an initial output of 20V, and a current limit of 200mA, turn on the bridge supply. Caution: If a Li-on battery is used instead of a regulated supply, it is recommended to add a 100uF or larger capacitor across the VBAT input terminal. This is necessary because the relatively large inductance of an Li-on battery may resonate with the bridge bypass capacitor resulting with excessive voltage.
6. Turn on the VDEN switch.
7. Measure 12V +/5% on the VDD pin of TB6 relative to the GND pin.
8. Turn on the VCEN switch.
9. Measure 3.3V ±3% on the VCC pin of TB6 relative to the GND pin.
10. Press the Start/Stop button. led0 is flashing.
11. Turn the potentiometer CW until the following waveform appears:



12. Confirm that the PWM frequency is 20kHz.
13. Turn off VCEN and VDEN switches. The HS output will stop switching.
14. Turn off the bridge supply
15. Move the J2 jumper from the 5V strap to the VCC strap. This configures the microcontroller to be powered from the VCC output of the HIP2104.
16. Turn on the bridge supply (still at 20V).

17. Turn on the VCEN switch. All 4 LEDs will flash one after another indicating power has been applied to the controller.
18. Press the Start/Stop button. The LI and HI inputs will start switching. (The HS output is not switching because VDD is off)
19. Turn on the VDen switch. HS is again switching.

Initial Setup to Evaluate the HIP2103 Daughter Card

The method to evaluate the HIP2103 is similar to the HIP2104 except that the VCC and VDD bias must be supplied from external bias supplies. TB6 is an output terminal for VCC and VDD when testing the HIP2104 but it is also an input terminal for VDD bias for the HIP2103. VCC on TB6 can also be used as a bias input for the microcontroller (or alternatively TB8).

DIP Switch Configuration for Testing with External Signals

It may be desirable to provide control signals from an off-board controller or logic generator.

1. Configure the DIP switch for external signals (all switches on). See Table 1.
2. Press the START/STOP button. Observe that led3 (EXTERNAL) is on.

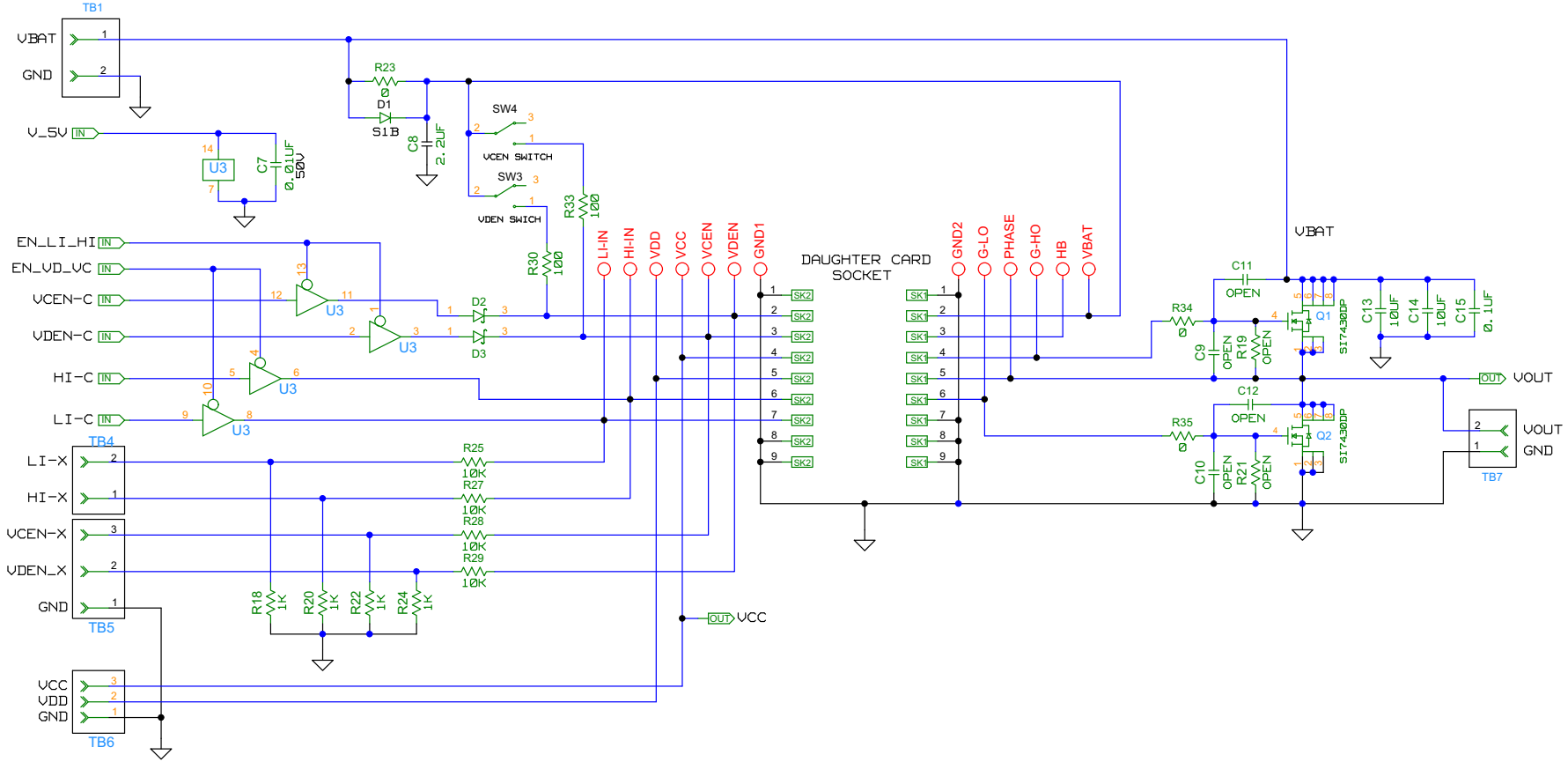
LED3 is on when configured for external inputs.

3. The U3 buffer on the mother board is now in the tri-state mode. All inputs, VCEN, VDEN, HI, LI must now come from an external controller. Terminal blocks GND_VDEN_VCEN (TB5), and HI_LI (TB4) are used for these inputs.

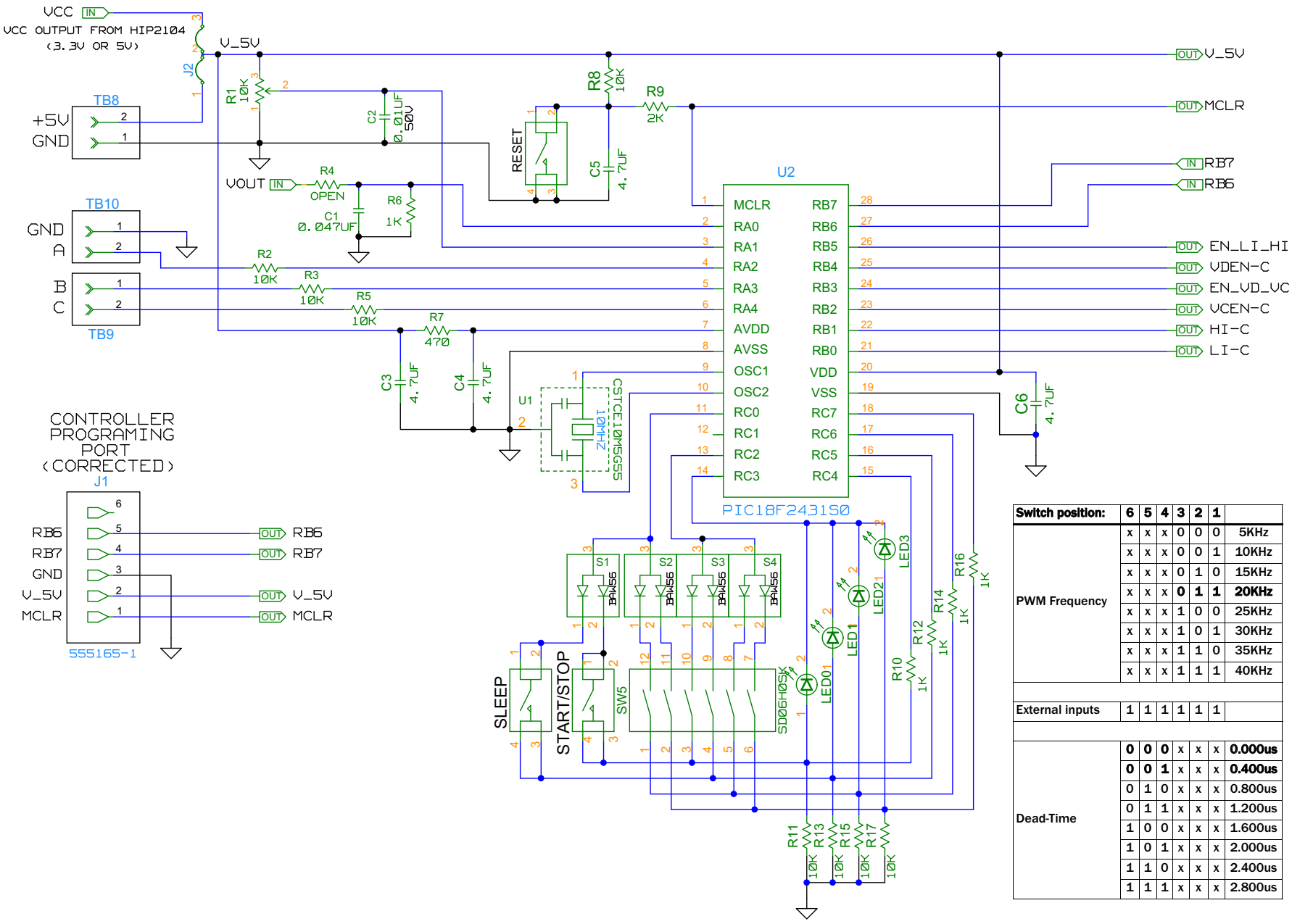
Related Literature

- FN8276 HIP2103, HIP2103 datasheet, “60V, 1A/2A MOSFET Driver”
- AN1899, “HIP2103_4DEMO1Z 3-phase BLDC Motor Drive”

Schematic, HIP2103_4MBEVAL1Z Bridge and Daughter Card Socket

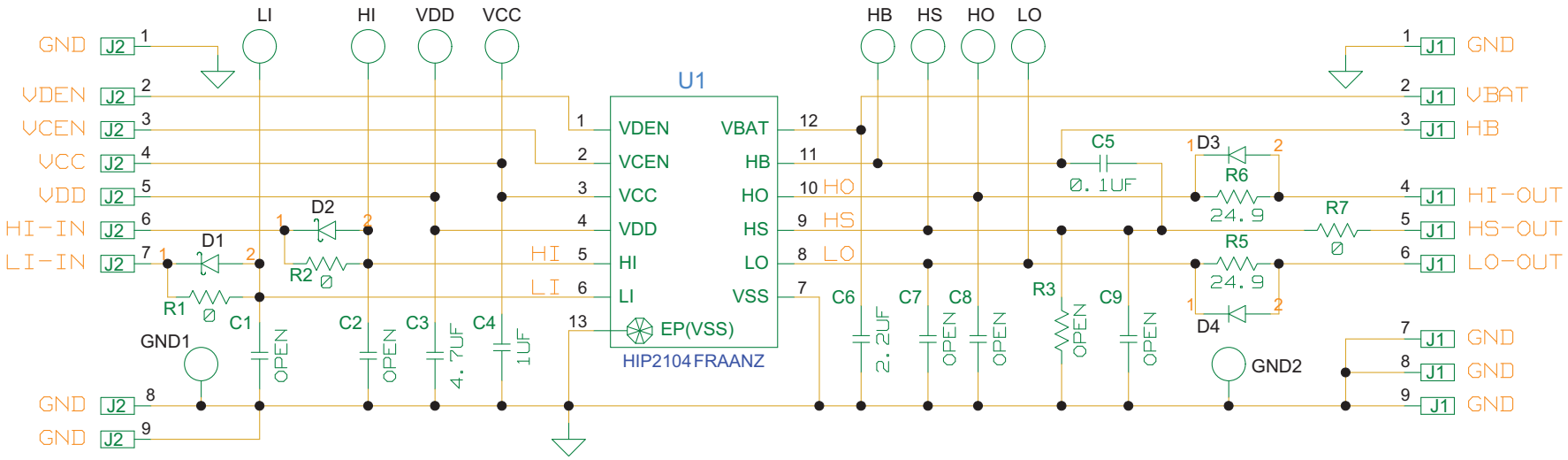


Schematic, HIP2103_4MBEVAL1Z Controller

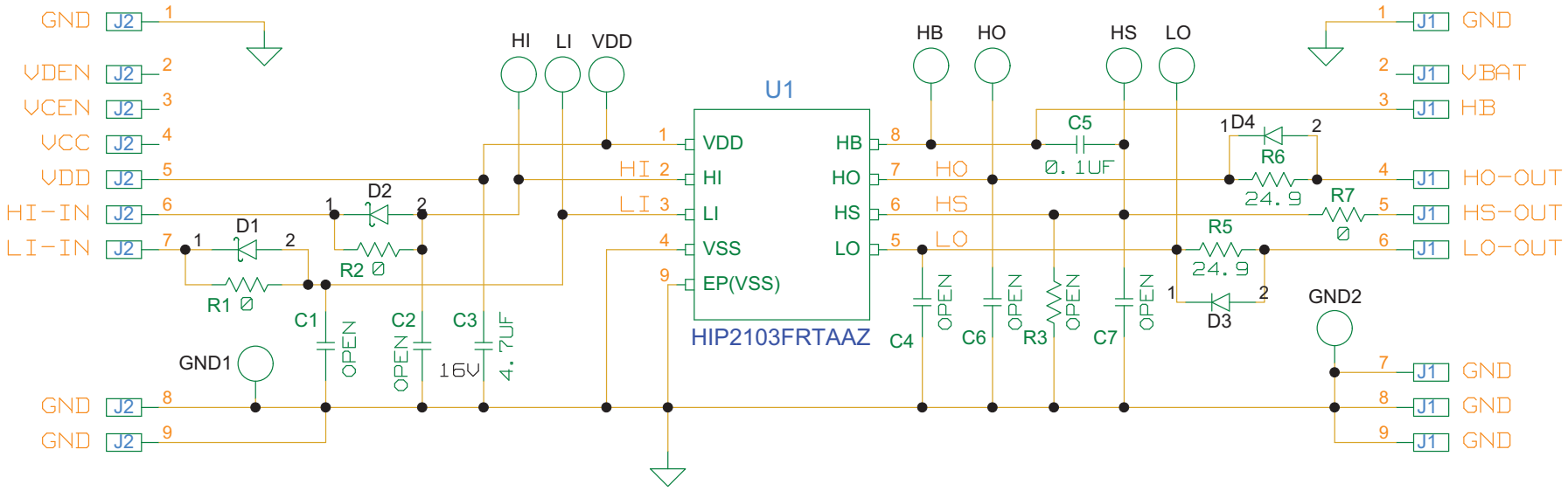


Switch position:	6	5	4	3	2	1	
PWM Frequency	x	x	x	0	0	0	5KHz
	x	x	x	0	0	1	10KHz
	x	x	x	0	1	0	15KHz
	x	x	x	**0**	**1**	**1**	**20KHz**
	x	x	x	1	0	0	25KHz
	x	x	x	1	0	1	30KHz
	x	x	x	1	1	0	35KHz
	x	x	x	1	1	1	40KHz
External inputs	1	1	1	1	1	1	
Dead-Time	**0**	**0**	**0**	x	x	x	**0.000us**
	0	**0**	**1**	x	x	x	**0.400us**
	0	1	0	x	x	x	0.800us
	0	1	1	x	x	x	1.200us
	1	0	0	x	x	x	1.600us
	1	0	1	x	x	x	2.000us
	1	1	0	x	x	x	2.400us
	1	1	1	x	x	x	2.800us

Schematic, HIP2104DBEVAL1Z Daughter Card



Schematic, HIP2103DBEVAL1Z Daughter Card



Board Layouts - PCB, HIP2103DBEVAL1Z

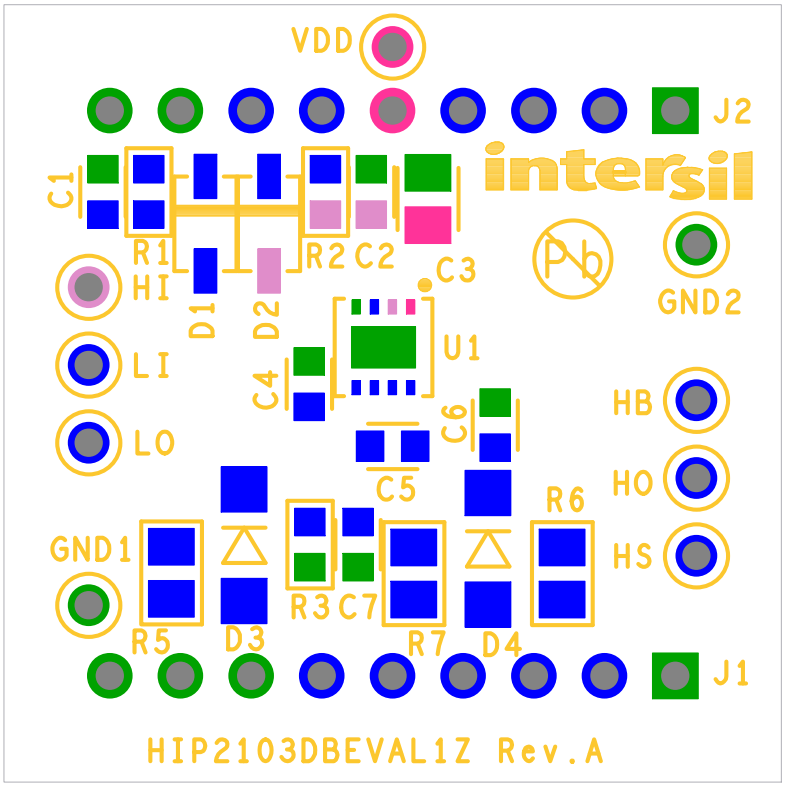


FIGURE 9. TOP SILKSCREEN

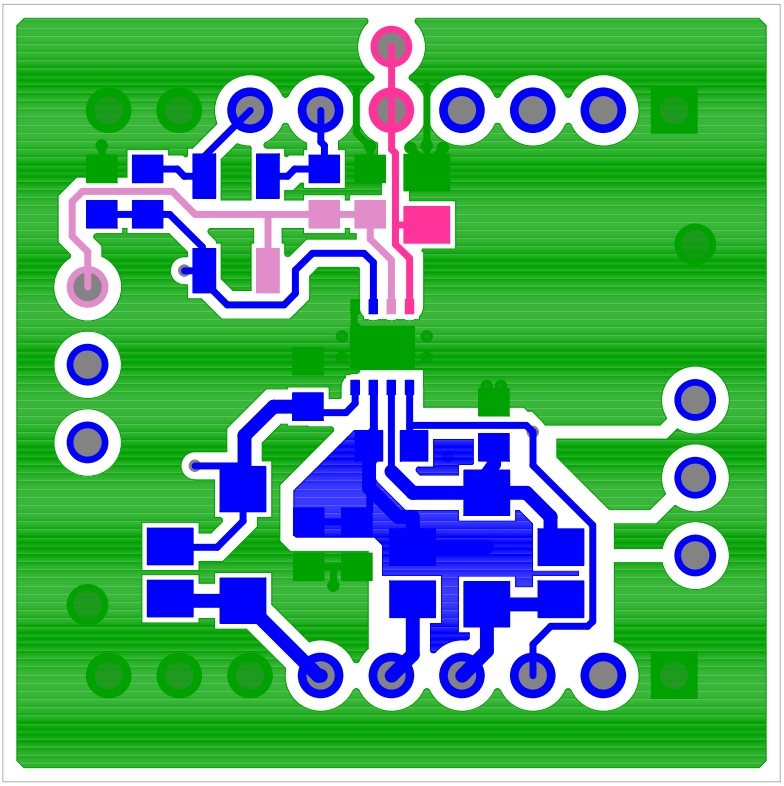


FIGURE 10. TOP LAYER

Board Layouts - PCB, HIP2103DBEVAL1Z (Continued)

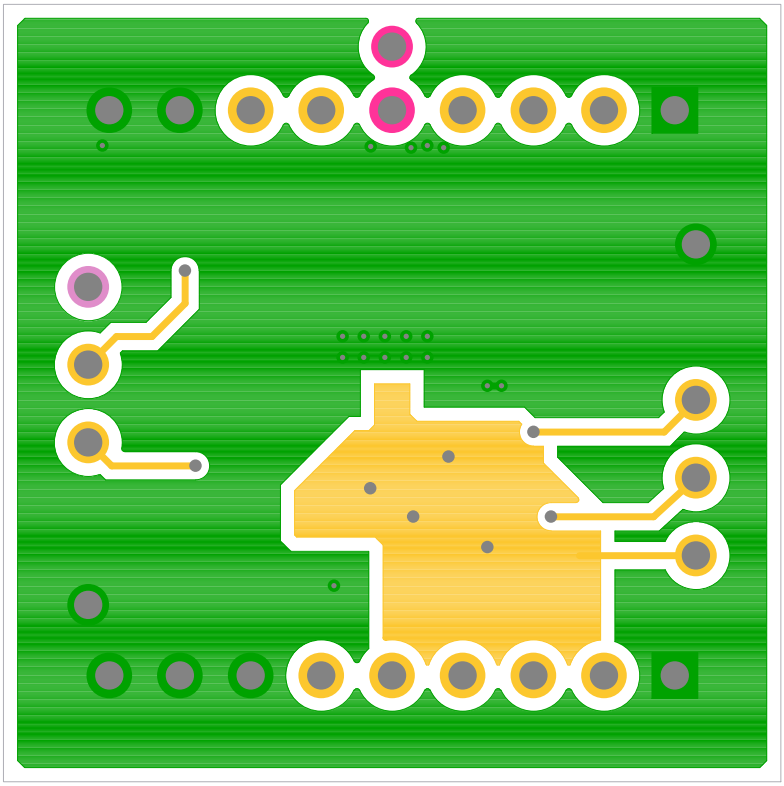


FIGURE 11. BOTTOM LAYER

BOM, HIP2103DBEVAL1Z

PART NUMBER	QTY	REF DES	MFR	DESCRIPTION
BAT54W-V	2	D1, D2	VISHAY	SMALL SIGNAL SCHOTTKY DIODE
BBL-109-G-E	2	J1, J2	SAMTEC	1 x 9 @ 0.1 SINGLE ROW
ES1A	2	D3, D4	FAIRCHILD	1A, 150V Fast Rectifier Diode
GRM21BR71C475KA73L	1	C3	MURATA	CERAMIC CAP
H1045-00104-25V10	1	C5	GENERIC	Multilayer Cap
H1045-OPEN	5	C1, C2, C4, C6, C7	GENERIC	Multilayer Cap
H2511-00R00-1/16W1	2	R1, R2	GENERIC	Thick Film Chip Resistor
H2511-ROPEN-OPEN	1	R3	GENERIC	Thick Film Chip Resistor
H2512-24R90-1/10W	2	R5, R6	GENERIC	Thick Film Chip Resistor
H2512-00R00-1/8W1	1	R7	GENERIC	Thick Film Chip Resistor
HIP2103FRTAAZ	1	U1	INTERSIL	60V Half Bridge Driver with 4V UVLO
TP_41C60P-DNP	9	HB, HI, HO, HS, LI, LO, VDD, GND1, GND2	GENERIC	Test Point 0.060 Pad 0.041 Thole (Do Not Populate)

Board Layouts - PCB, HIP2104DBEVAL1Z

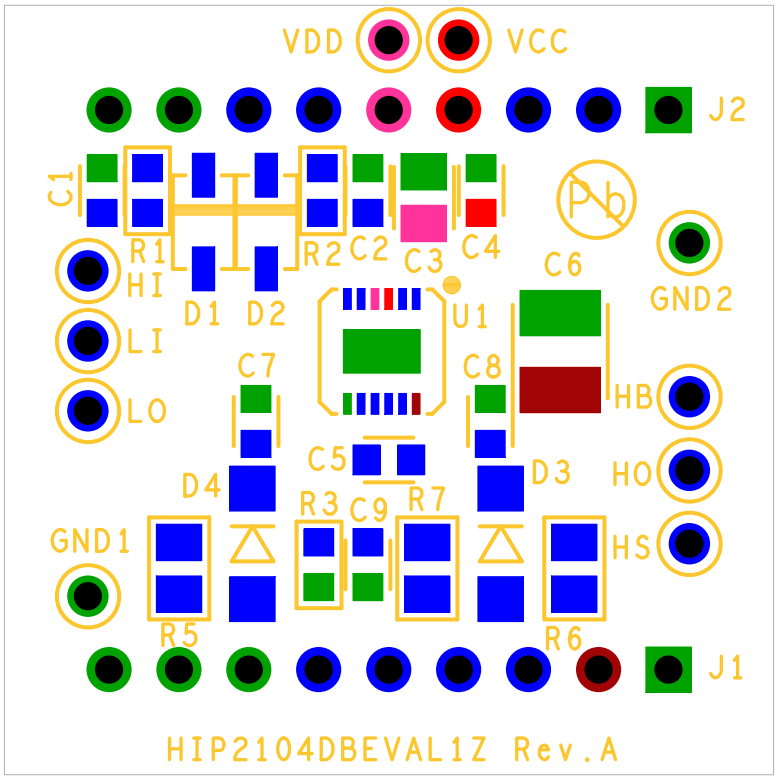


FIGURE 12. TOP SILKSCREEN

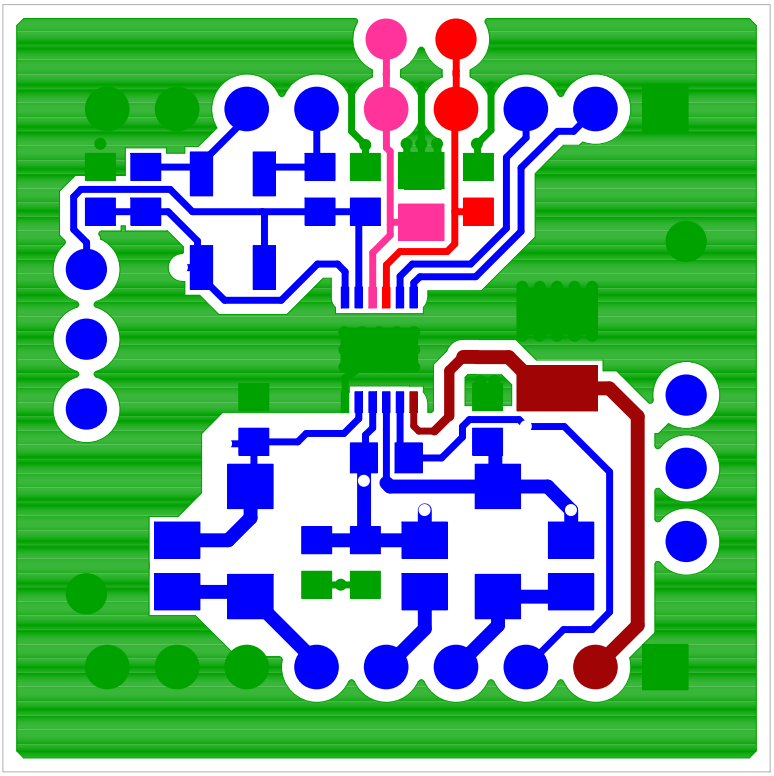


FIGURE 13. TOP LAYER

Board Layouts - PCB, HIP2104DBEVAL1Z (Continued)

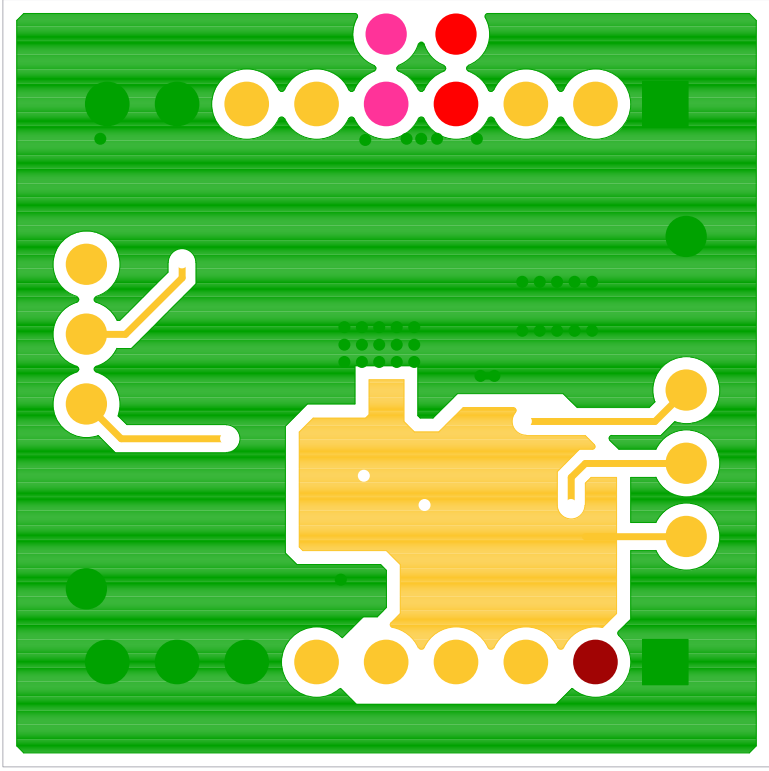


FIGURE 14. BOTTOM LAYER

BOM, HIP2104DBEVAL1Z

PART NUMBER	QTY	REF DES	MFR	DESCRIPTION
BAT54W-V	2	D1, D2	VISHAY	SMALL SIGNAL SCHOTTKY DIODE
BBL-109-G-E	2	J1, J2	SAMTEC	1 x 9 @ 0.1 SINGLE ROW
C1608X7R1C105K	1	C4	TDK	MULTILAYER CAP
ES1A	2	D3, D4	FAIRCHILD	1A, 150V Fast Rectifier Diode
GRM21BR71C475KA73L	1	C3	MURATA	CERAMIC CAP
H1045-00104-25V10	1	C5	GENERIC	Multilayer Cap
H1045-OPEN	5	C1, C2, C7, C8, C9	GENERIC	Multilayer Cap
H1082-00225-100V10	1	C6	GENERIC	Ceramic Chip Cap
H2511-00R00-1/16W1	2	R1, R2	GENERIC	Thick Film Chip Resistor
H2511-ROPEN-OPEN	1	R3	GENERIC	Thick Film Chip Resistor
H2512-24R90-1/10W	2	R5, R6	GENERIC	Thick Film Chip Resistor
H2512-00R00-1/8W1	1	R7	GENERIC	Thick Film Chip Resistor
HIP2104FRAANZ	1	U1	INTERSIL	60V Half Bridge Driver with 4V UVLO
TP_41C60P-DNP	10	HB, HI, HO, HS, LI, LO, VCC, VDD, GND1, GND2	GENERIC	Test Point 0.060 Pad 0.041 Thole (Do Not Populate)

PCB, HIP2103_4MBEVAL1Z

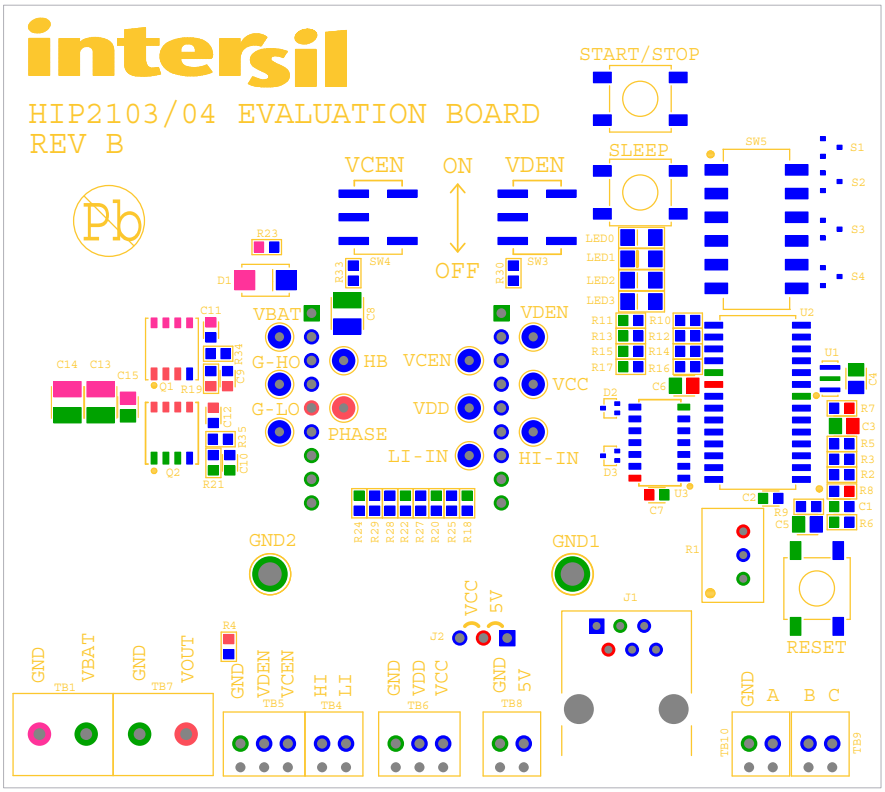


FIGURE 15. TOP SILKSCREEN

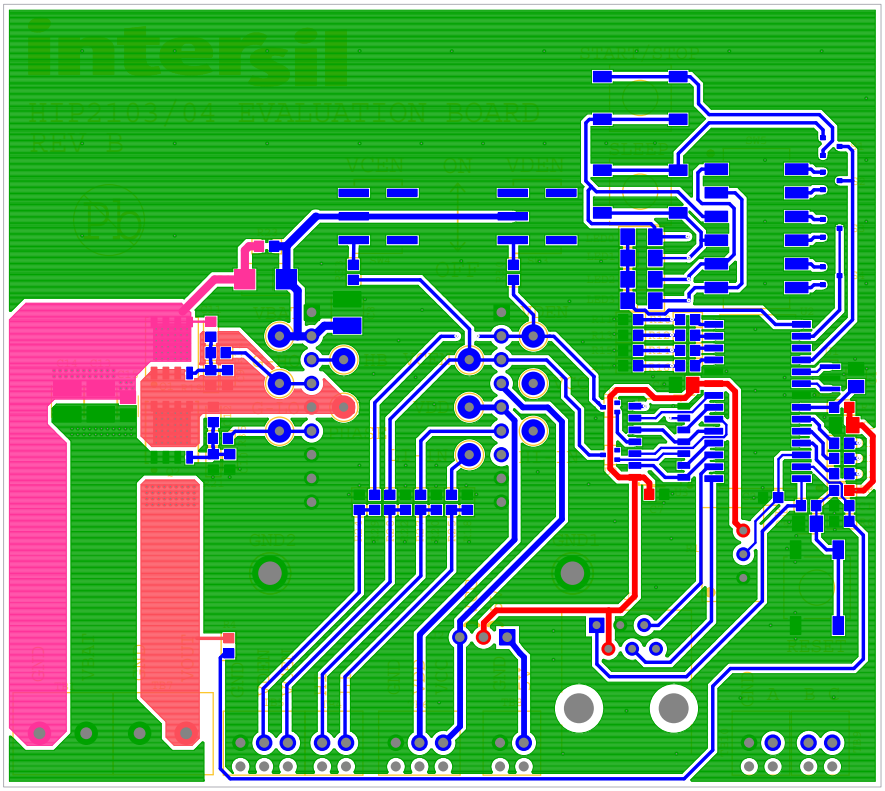


FIGURE 16. TOP LAYER

PCB, HIP2103_4MBEVAL1Z (Continued)

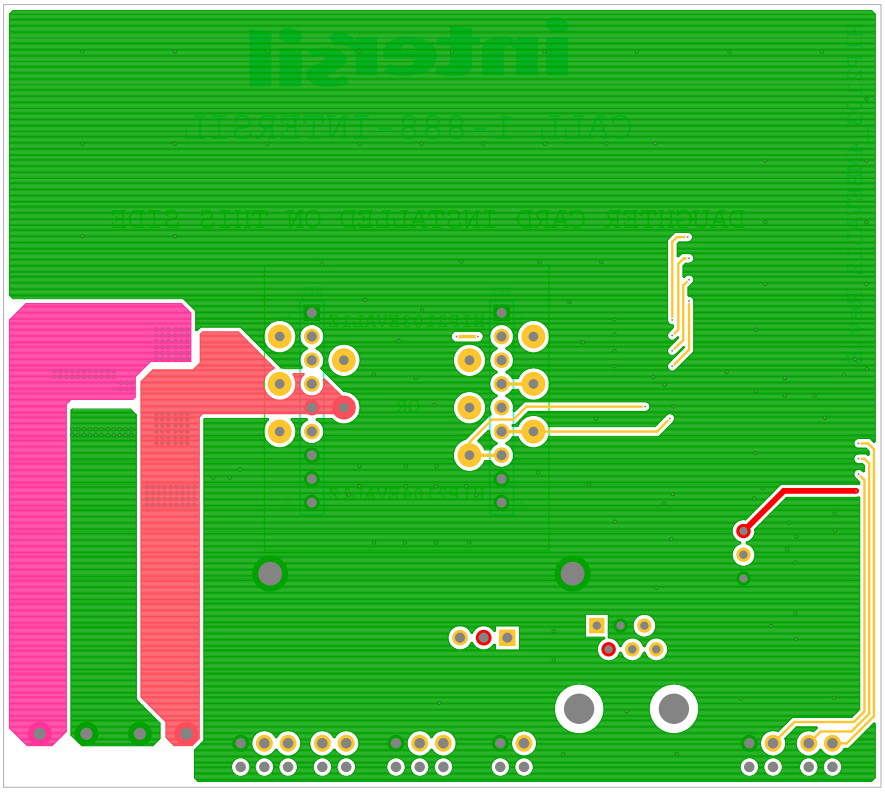


FIGURE 17. BOTTOM LAYER

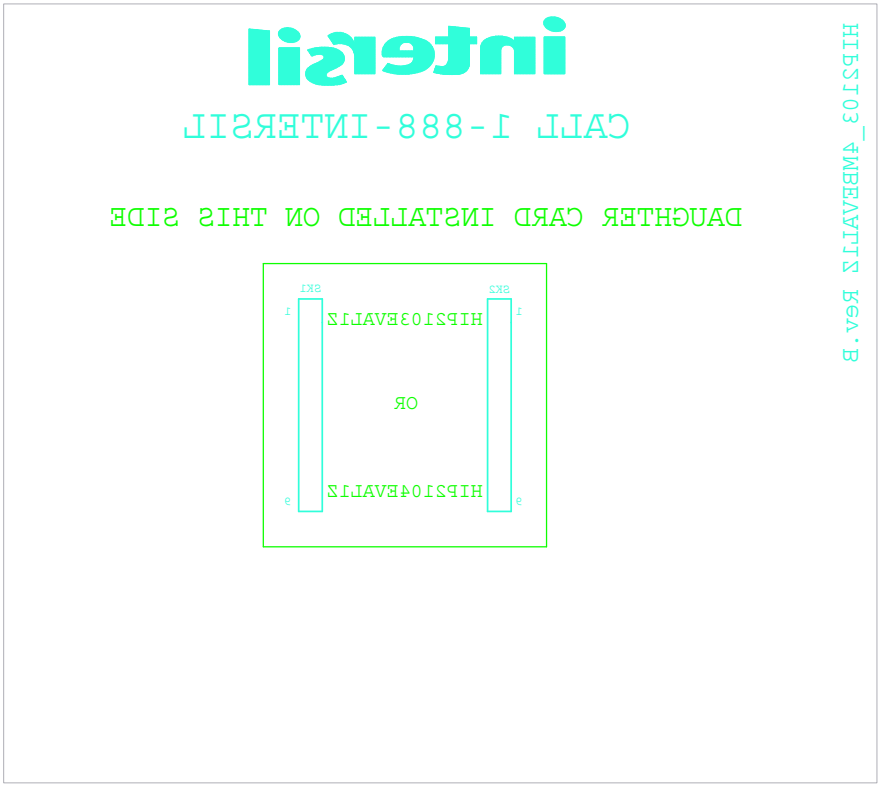


FIGURE 18. BOTTOM SILKSCREEN

BOM, HIP2103_4MBEVAL1Z

PART NUMBER	QTY	REF DES	MANUFACTURER	DESCRIPTION
1514-2	2	GND1, GND2	KEYSTONE	Test Point Turret 0.150 Pad 0.100 Thole
1725656	4	TB4, TB8-TB10	PHOENIX-CONTACT	100 Mil Micro-Pitch Terminal Block
1725669	2	TB5, TB6	PHOENIX-CONTACT	100 Mil Micro-Pitch Terminal Block
1729018	2	TB1, TB7	PHOENIX-CONTACT	200 Mil PCB Connector Terminal Block
3299W-1-103-LF	1	R1	BOURNS	TRIMMER POTENTIOMETER (RoHS COMPLIANT)
5000	11	HB, VCC, VDD, G-HO, G-LO, VBAT, VCEN, VDEN, HI-IN, LI-IN, PHASE	KEYSTONE	Miniature Red Test Point 0.100 Pad 0.040 Thole
555165-1	1	J1	TYCO	Phone Jack Connector
597-3111-402	4	LED0-LED3	Dialight	Surface Mount Red LED
B3S-1002	3	RESET, SLEEP, START/STOP	OMRON	Momentary Pushbutton Tactile SMT Switch
BAS70T-7-F	2	D2, D3	DIODES	70V, 150mW SCHOTTKY BARRIER DIODE
BAW56	4	S1-S4	RECTRON-SEMI	Dual 1N4148 Common Anode Diode
C3225X7S1H106K	2	C13, C14	TDK	Ceramic Chip Cap
CD74HC125M	1	U3	Texas Instruments	Quad Tri-State Buffer
CONN-1X9	2	SK1, SK2	Generic	Inline 9 pins x 0.1 inch Connector Strip
CSTCE10M5G55	1	U1	MURATA	Piezoelectric Resonator
GRM21BR71C475KA73L	4	C3-C6	MURATA	CERAMIC CAP
GT11MSCBETR	2	SW3, SW4	C&K	SPDT On-None-On SM Ultraminiature Toggle Switch
H1045-00103-50V10	2	C2, C7	GENERIC	Multilayer Cap
H1045-00473-25V10	1	C1	GENERIC	Multilayer Cap
H1045-OPEN	4	C9-C12	GENERIC	Multilayer Cap
H1046-00104-50V10	1	C15	GENERIC	Multilayer Cap
H1082-00225-100V10	1	C8	GENERIC	Ceramic Chip Cap
H2511-00R00-1/16W	3	R23, R34, R35	GENERIC	Thick Film Chip Resistor
H2511-01000-1/16W1	2	R30, R33	GENERIC	Thick Film Chip Resistor
H2511-01001-1/16W1	9	R6, R10, R12, R14, R16, R18, R20, R22, R24	GENERIC	Thick Film Chip Resistor
H2511-01002-1/10W1	4	R25, R27-R29	GENERIC	Thick Film Chip Resistor
H2511-01002-1/16W1	8	R2, R3, R5, R8, R11, R13, R15, R17	GENERIC	Thick Film Chip Resistor
H2511-02001-1/16W1	1	R9	GENERIC	Thick Film Chip Resistor
H2511-04700-1/16W1	1	R7	GENERIC	Thick Film Chip Resistor
H2511-ROPEN-OPEN	3	R4, R19, R21	GENERIC	Thick Film Chip Resistor
JUMPER-3-100	1	J2	GENERIC	Three Pin Jumper
PIC18F2431S0	1	U2	Microchip	Flash Microcontroller
S1B	1	D1	VISHAY	1A, 100V Generic Rectifier Diode
SD06H0SK	1	SW5	C&K	SD Series Low Profile DIP Switch 6 Pos SPST
SI7430DP	2	Q1, Q2	VISHAY	N-Channel 150V, 26A WFET