



CYPRESS

CY2280

100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum for Mobile or Desktop PCs

Features

- **Mixed 2.5V and 3.3V operation**
- **Clock solution for Pentium® II, and other similar processor-based motherboards**
 - Four 2.5V CPU clocks up to 100 MHz
 - Eight 3.3V sync. PCI clocks, one free-running
 - Two 3.3V 48-MHz USB clocks
 - Three 3.3V Ref. clocks at 14.318 MHz
 - Two 2.5V APIC clocks at 14.318 MHz or PCI/2
- **EMI control**
 - Spread spectrum clocking
 - Factory-EPROM programmable spread spectrum margin
 - Factory-EPROM programmable output drive and slew rate
- **Factory-EPROM programmable CPU clock frequencies for custom configurations**
- **Available in space-saving 48-pin SSOP package**

Functional Description

The CY2280 is a Spread Spectrum clock synthesizer/driver for a Pentium II, or other similar processor-based PC requiring 100-MHz support. All of the required system clocks are provided in a space-saving 48-pin SSOP package. The CY2280 can be used with the CY231x for a total solution for systems with SDRAM.

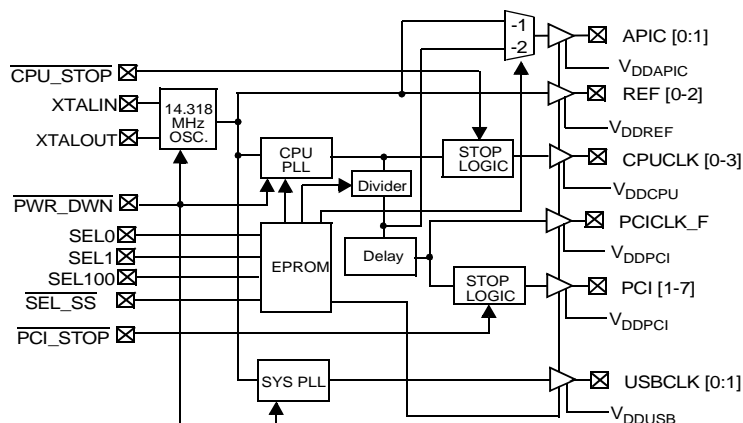
The CY2280 provides the option of spread spectrum clocking on the CPU and PCI clocks for reduced EMI. A downspread percentage is introduced when the SEL_SS input is asserted. The device can be run without spread spectrum when the SEL_SS input is deasserted. The percentage of spreading is EPROM-programmable to optimize EMI-reduction.

The CY2280 has power-down, CPU stop, and PCI stop pins for power management control. The signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the CPU_STOP input is asserted, the CPU clock outputs are driven LOW. When the PCI_STOP input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the PWR_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

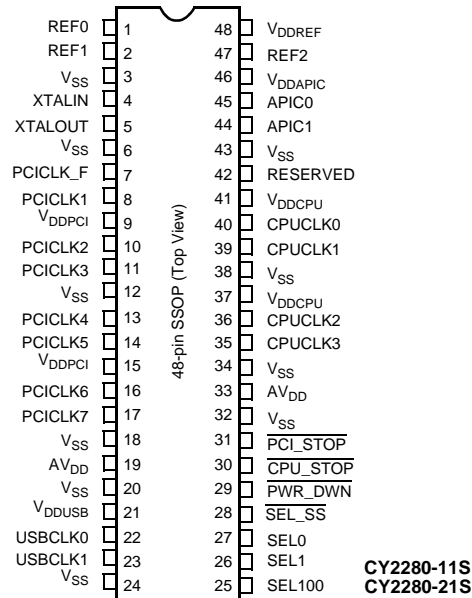
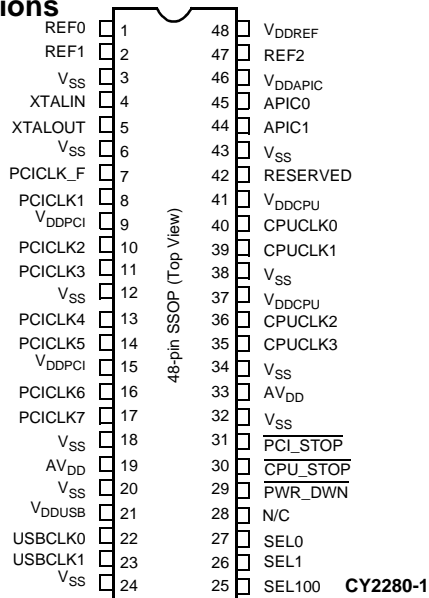
CY2280 Selector Guide

| Clock Outputs | CY2280 Configuration Options | | |
|------------------------------|------------------------------|------------|------------|
| | -1 | -11S | -21S |
| CPU (66.6, 100 MHz) | 4 | 4 | 4 |
| PCI (CPU/2, CPU/3) | 8 | 8 | 8 |
| USB (48 MHz) | 2 | 2 | 2 |
| APIC (14.318 MHz) | 2 | 2 | — |
| APIC (PCI/2) | — | — | 2 |
| Reference (14.318 MHz) | 3 | 3 | 3 |
| CPU-PCI delay | 1.5–4.0 ns | 1.5–4.0 ns | 1.5–4.0 ns |
| CPU-APIC delay | — | — | 2.0–4.5 ns |
| Spread Spectrum (Downspread) | N/A | -0.6% | -0.6% |

Logic Block Diagram



Pentium is a registered trademark of Intel Corporation.

Pin Configurations

Pin Summary

| Name | Pins | Description |
|------------------------|--------------------------------------|---|
| VDDPCI | 15, 9 | 3.3V Digital voltage supply for PCI clocks |
| VDDUSB | 21 | 3.3V Digital voltage supply for USB clocks |
| VDDREF | 48 | 3.3V Digital voltage supply for REF clocks |
| VDDAPIC | 46 | 2.5V Digital voltage supply for APIC clocks |
| VDDCPU | 41, 37 | 2.5V Digital voltage supply for CPU clocks |
| AV _{DD} | 33, 19 | Analog voltage supply, 3.3V |
| V _{SS} | 3, 6, 12, 18, 20, 24, 32, 34, 38, 43 | Ground |
| XTALIN ^[1] | 4 | Reference crystal input |
| XTALOUT ^[1] | 5 | Reference crystal feedback |
| PCI_STOP | 31 | Active LOW control input to stop PCI clocks |
| CPU_STOP | 30 | Active LOW control input to stop CPU clocks |
| PWR_DWN | 29 | Active LOW control input to power down device |
| SEL_SS | 28 | Spread spectrum select input (-11S and -21S options) |
| N/C | 28 | Spread spectrum select input (-1 option) |
| SEL0 | 27 | CPU frequency select input, bit 0 (see Function Table) |
| SEL1 | 26 | CPU frequency select input, bit 1 (see Function Table) |
| SEL100 | 25 | CPU frequency select input, selects between 100 MHz and 66.6 MHz (see Function Table) |
| CPUCLK[0:3] | 40, 39, 36, 35 | CPU clock outputs |
| PCICLK[1:7] | 8, 10, 11, 13, 14, 16, 17 | PCI clock outputs, at one-half or one-third the CPU frequency of 66.6 MHz or 100 MHz respectively |
| PCICLK_F | 7 | Free-running PCI clock output |
| APIC[0:1] | 45, 44 | APIC clock outputs |
| REF[0:2] | 1, 2, 47 | 3.3V Reference clock outputs |
| USBCLK[0:1] | 22, 23 | USB clock outputs |
| RESERVED | 42 | Reserved |

Note:

- For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Function Table (-11S Option)

| SEL100 | SEL1 | SEL0 | $\overline{\text{SEL_SS}}^{[2]}$ | CPU/PCI Ratio | CPUCLK | PCICLK_F PCICLK | REF | APIC | USBCLK |
|--------|------|------|-----------------------------------|---------------|-----------|--------------------|---------------------|---------------------|--------|
| 0 | 0 | 0 | N/A | 2 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 0 | 0 | 1 | N/A | 2 | Reserved | Reserved | 14.318 MHz | 14.318 MHz | 48 MHz |
| 0 | 1 | 0 | N/A | 2 | Reserved | Reserved | 14.318 MHz | 14.318 MHz | 48 MHz |
| 0 | 1 | 1 | 0 (downspread) | 2 | 66.66 MHz | 33.33 MHz | 14.318 MHz | 14.318 MHz | 48 MHz |
| 0 | 1 | 1 | 1 (no spread) | 2 | 66.66 MHz | 33.33 MHz | 14.318 MHz | 14.318 MHz | 48 MHz |
| 1 | 0 | 0 | N/A | 3 | TCLK/2 | TCLK/6 | TCLK ^[3] | TCLK ^[3] | TCLK/2 |
| 1 | 0 | 1 | N/A | 3 | Reserved | Reserved | 14.318 MHz | 14.318 MHz | 48 MHz |
| 1 | 1 | 0 | N/A | 3 | Reserved | Reserved | 14.318 MHz | 14.318 MHz | 48 MHz |
| 1 | 1 | 1 | 0 (downspread) | 3 | 100 MHz | 33.33 MHz | 14.318 MHz | 14.318 MHz | 48 MHz |
| 1 | 1 | 1 | 1 (no spread) | 3 | 100 MHz | 33.33 MHz | 14.318 MHz | 14.318 MHz | 48 MHz |

Function Table (-21S Option)

| SEL100 | SEL1 | SEL0 | $\overline{\text{SEL_SS}}^{[2]}$ | CPU/PCI Ratio | CPUCLK | PCICLK_F PCICLK | REF | APIC | USBCLK |
|--------|------|------|-----------------------------------|---------------|-----------|--------------------|---------------------|------------------------|--------|
| 0 | 0 | 0 | N/A | 2 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 0 | 0 | 1 | N/A | 2 | Reserved | Reserved | 14.318 MHz | Reserved | 48 MHz |
| 0 | 1 | 0 | N/A | 2 | Reserved | Reserved | 14.318 MHz | Reserved | 48 MHz |
| 0 | 1 | 1 | 0 (downspread) | 2 | 66.66 MHz | 33.33 MHz | 14.318 MHz | 16.67 MHz | 48 MHz |
| 0 | 1 | 1 | 1 (no spread) | 2 | 66.66 MHz | 33.33 MHz | 14.318 MHz | 16.67 MHz | 48 MHz |
| 1 | 0 | 0 | N/A | 3 | TCLK/2 | TCLK/6 | TCLK ^[3] | TCLK/12 ^[3] | TCLK/2 |
| 1 | 0 | 1 | N/A | 3 | Reserved | Reserved | 14.318 MHz | Reserved | 48 MHz |
| 1 | 1 | 0 | N/A | 3 | Reserved | Reserved | 14.318 MHz | Reserved | 48 MHz |
| 1 | 1 | 1 | 0 (downspread) | 3 | 100 MHz | 33.33 MHz | 14.318 MHz | 16.67 MHz | 48 MHz |
| 1 | 1 | 1 | 1 (no spread) | 3 | 100 MHz | 33.33 MHz | 14.318 MHz | 16.67 MHz | 48 MHz |

Actual Clock Frequency Values

| Clock Output | Target Frequency (MHz) | Actual Frequency (MHz) | PPM |
|--------------|------------------------|------------------------|-------|
| CPUCLK | 66.67 | 66.654 | -195 |
| CPUCLK | 100 | 99.77 | -2346 |
| USBCLK | 48.0 | 48.008 | 167 |

Power Management Logic

| $\overline{\text{CPU_STOP}}$ | $\overline{\text{PCI_STOP}}$ | $\overline{\text{PWR_DWN}}$ | CPUCLK | PCICLK | PCICLK_F | Other Clocks | Osc. | PLLs |
|-------------------------------|-------------------------------|------------------------------|---------|---------|----------|--------------|---------|---------|
| X | X | 0 | Low | Low | Low | Low | Off | Off |
| 0 | 0 | 1 | Low | Low | Running | Running | Running | Running |
| 0 | 1 | 1 | Low | Running | Running | Running | Running | Running |
| 1 | 0 | 1 | Running | Low | Running | Running | Running | Running |
| 1 | 1 | 1 | Running | Running | Running | Running | Running | Running |

Notes:

- Target frequency is modulated by percentage shown (max.) when $\overline{\text{SEL_SS}} = 0$.
- TCLK supplied on the XTALIN pin in Test Mode.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to + 7.0V
 Input Voltage -0.5V to $V_{DD} + 0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C
 Junction Temperature +150°C
 Package Power Dissipation 1W
 Static Discharge Voltage > 2000V
 (per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions^[4]

| Parameter | Description | Min. | Max. | Unit |
|--|--|--------|----------------------|------|
| AV_{DD} , V_{DDPCI} , V_{DDUSB} , V_{DDREF} | Analog and Digital Supply Voltage | 3.135 | 3.465 | V |
| V_{DDCPU} | CPU Supply Voltage | 2.375 | 2.625 | V |
| V_{DDAPIC} | APIC Supply Voltage | 2.375 | 2.625 | V |
| T_A | Operating Temperature, Ambient | 0 | 70 | °C |
| C_L | Max. Capacitive Load on CPUCLK PCICLK APIC, REF USB | | 20 30 20 20 | pF |
| $f_{(REF)}$ | Reference Frequency, Oscillator Nominal Value | 14.318 | 14.318 | MHz |
| t_{PU} | Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|------------|---|--|------|------|------|
| V_{IH} | High-level Input Voltage | Except Crystal Inputs ^[5] | 2.0 | | V |
| V_{IL} | Low-level Input Voltage | Except Crystal Inputs ^[5] | | 0.8 | V |
| V_{OH} | High-level Output Voltage ^[6] | $V_{DDCPU} = V_{DDAPIC} = 2.375V$ $I_{OH} = 12\text{ mA}$ CPUCLK $I_{OH} = 18\text{ mA}$ APIC | 2.0 | | V |
| V_{OL} | Low-level Output Voltage ^[6] | $V_{DDCPU} = V_{DDAPIC} = 2.375V$ $I_{OL} = 12\text{ mA}$ CPUCLK $I_{OL} = 18\text{ mA}$ APIC | | 0.4 | V |
| V_{OH} | High-level Output Voltage ^[6] | $V_{DDPCI}, AV_{DD}, V_{DDREF}, V_{DDUSB} = 3.135V$ $I_{OH} = 14.5\text{ mA}$ PCICLK $I_{OH} = 16\text{ mA}$ USBCLK $I_{OH} = 16\text{ mA}$ REF | 2.4 | | V |
| V_{OL} | Low-level Output Voltage ^[6] | $V_{DDPCI}, AV_{DD}, V_{DDREF}, V_{DDUSB} = 3.135V$ $I_{OL} = 9.4\text{ mA}$ PCICLK $I_{OL} = 9\text{ mA}$ USBCLK $I_{OL} = 9\text{ mA}$ REF | | 0.4V | V |
| I_{IH} | Input High Current | $V_{IH} = V_{DD}$ | -10 | +10 | μA |
| I_{IL} | Input Low Current | $V_{IL} = 0V$ | | 10 | μA |
| I_{OZ} | Output Leakage Current | Three-state | -10 | +10 | μA |
| I_{DD25} | Power Supply Current for 2.5V Clocks ^[6] | $V_{DDCPU} = 2.625V$, $V_{IN} = 0$ or V_{DD} , Loaded Outputs, CPU = 66.6 MHz | | 70 | mA |
| I_{DD25} | Power Supply Current for 2.5V Clocks ^[6] | $V_{DDCPU} = 2.625V$, $V_{IN} = 0$ or V_{DD} , Loaded Outputs, CPU = 100 MHz | | 100 | mA |
| I_{DD33} | Power Supply Current for 3.3V Clocks ^[6] | $V_{DD} = 3.465V$, $V_{IN} = 0$ or V_{DD} , Loaded Outputs | | 170 | mA |
| I_{DDS} | Power-down Current ^[6] | Current draw in power-down state | | 500 | μA |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------|-------------|-----------------|------|------|------|
|-----------|-------------|-----------------|------|------|------|

Notes:

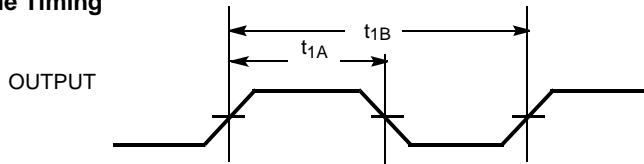
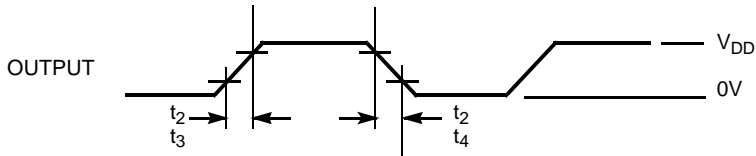
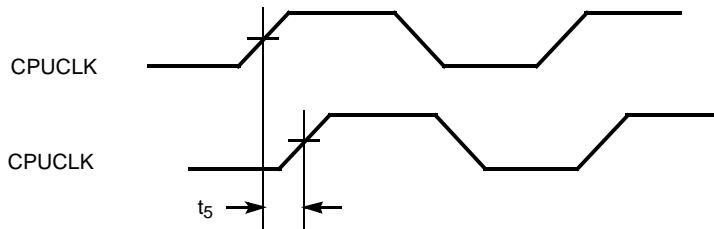
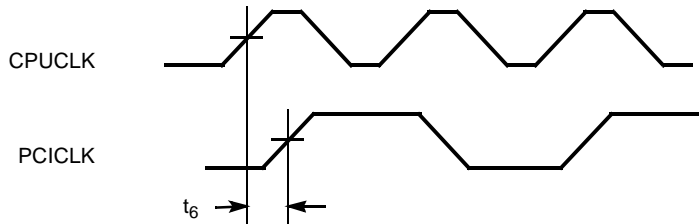
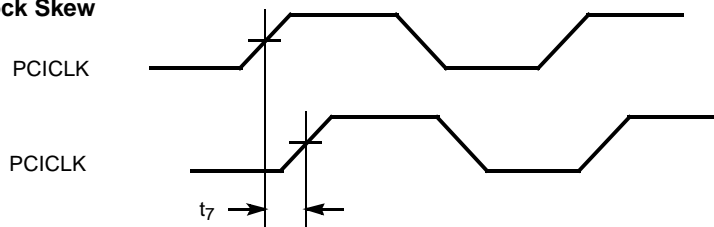
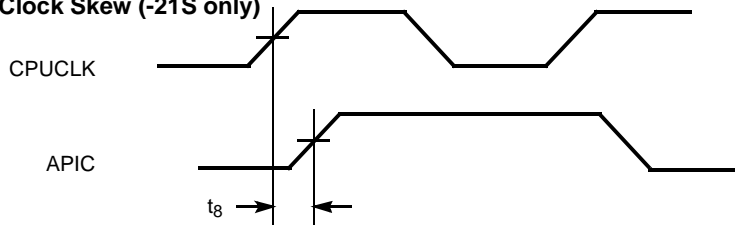
4. Electrical parameters are guaranteed with these operating conditions.
5. Crystal Inputs have CMOS thresholds.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

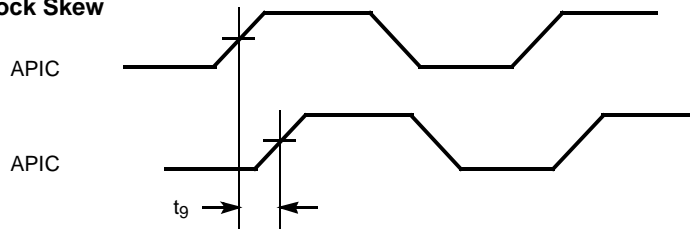
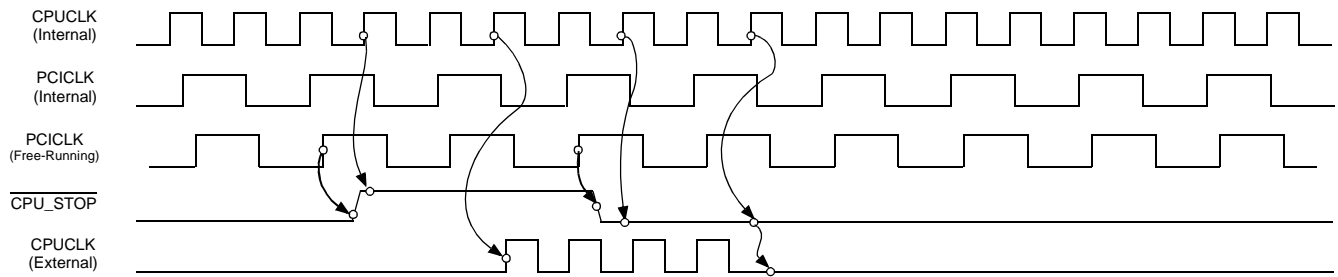
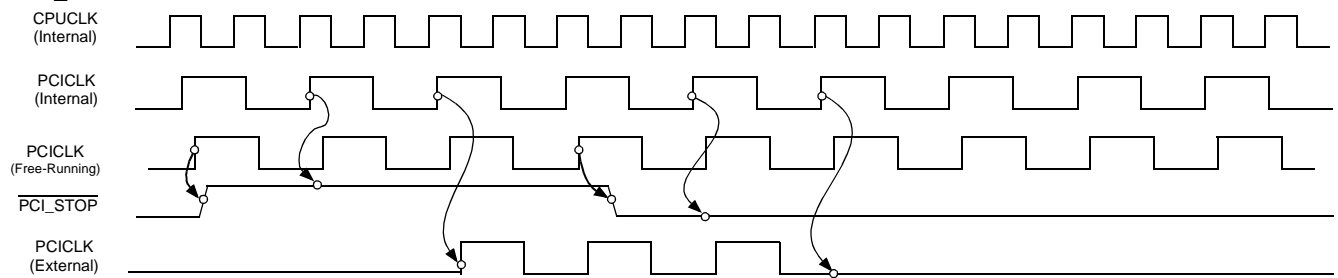
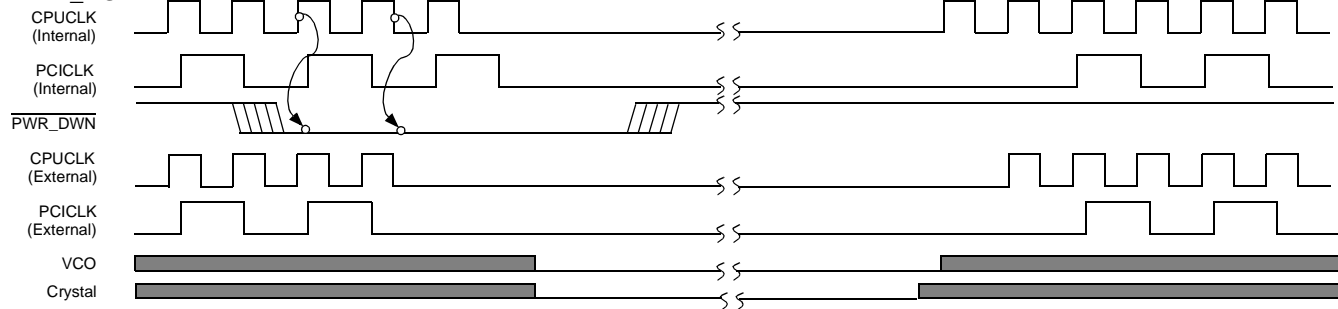
Switching Characteristics^[6, 7]

| Parameter | Output | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------|----------------|---|--|------|------|------|------|
| t ₁ | All | Output Duty Cycle ^[8] | $t_1 = t_{1A} \div t_{1B}$ | 45 | 50 | 55 | % |
| t ₂ | CPUCLK, APIC | CPU and APIC Clock Rising and Falling Edge Rate | Between 0.4V and 2.0V -1,-11S, -21S | 1.0 | | 4.0 | V/ns |
| t ₂ | PCICLK | PCI Clock Rising and Falling Edge Rate | Between 0.4V and 2.4V -1,-11S, -21S | 1.0 | | 4.0 | V/ns |
| t ₂ | USBCLK, REF | USB, REF Rising and Falling Edge Rate | Between 0.4V and 2.4V | 0.5 | | 2.0 | V/ns |
| t ₃ | CPUCLK | CPU Clock Rise Time | Between 0.4V and 2.0V -1,-11S, -21S | 0.4 | | 1.6 | ns |
| t ₄ | CPUCLK | CPU Clock Fall Time | Between 2.0V and 0.4V -1,-11S, -21S | 0.4 | | 1.6 | ns |
| t ₅ | CPUCLK | CPU-CPU Clock Skew | Measured at 1.25V | | 100 | 175 | ps |
| t ₆ | CPUCLK, PCICLK | CPU-PCI Clock Skew ^[9] | Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks -1,-11S, -21S | 1.5 | | 4.0 | ns |
| t ₇ | PCICLK, PCICLK | PCI-PCI Clock Skew | Measured at 1.5V | | | 250 | ps |
| t ₈ | CPUCLK, APIC | CPU-APIC Clock Skew ^[10] | Measured at 1.25V for 2.5V clocks -21S | 2.0 | | 4.5 | ns |
| t ₉ | APIC | APIC-APIC Clock Skew | Measured at 1.25V | | 100 | 175 | ps |
| t ₁₀ | CPUCLK | Cycle-Cycle Clock Jitter | Measured at 1.25V -1,-11S, -21S | | 200 | 250 | ps |
| t ₁₁ | PCICLK | Cycle-Cycle Clock Jitter | Measured at 1.5V | | 250 | 500 | ps |
| t ₁₂ | CPUCLK, PCICLK | Power-up Time | CPU, PCI clock stabilization from power-up | | | 3 | ms |

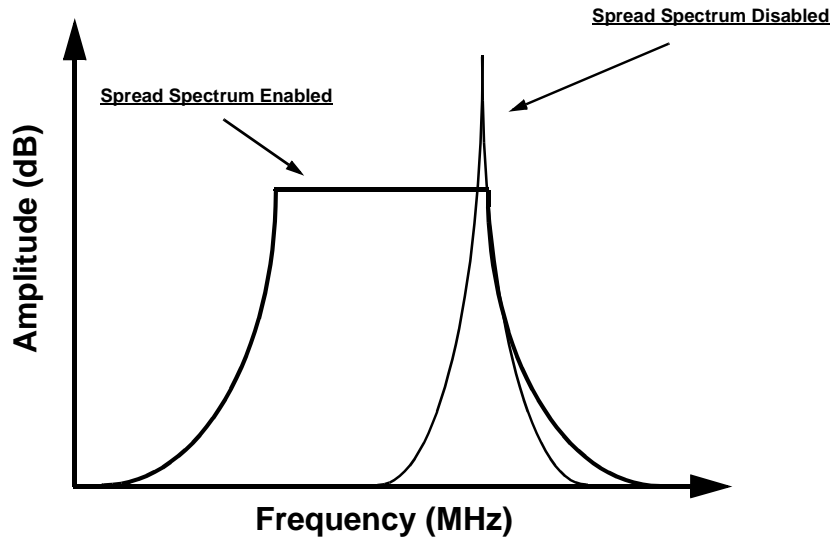
Notes:

7. All parameters specified with loaded outputs.
8. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
9. PCI lags CPU for -11S and -21S options.
10. APIC lags CPU for -21S option.

Switching Waveforms
Duty Cycle Timing

All Outputs Rise/Fall Time

CPU-CPU Clock Skew

CPU-PCI Clock Skew

PCI-PCI Clock Skew

CPU-APIC Clock Skew (-21S only)


Switching Waveforms (continued)
APIC-APIC Clock Skew

CPU_STOP

PCI_STOP

PWR_DOWN


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

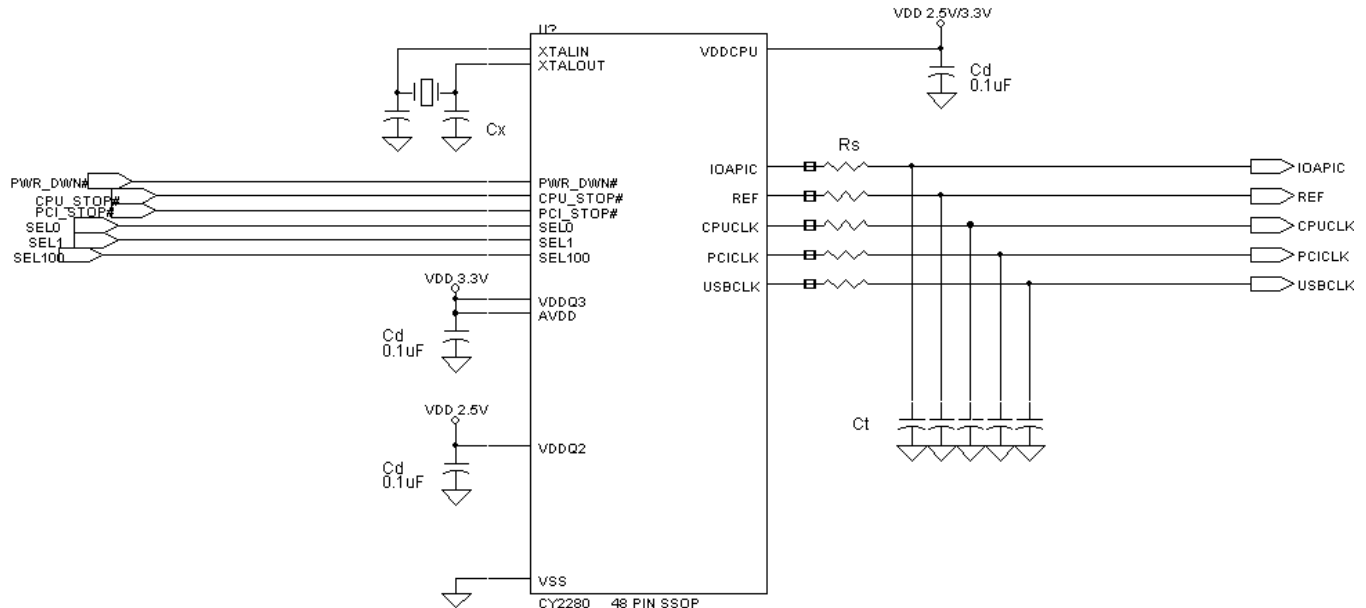
Spread Spectrum Clocking


| Description | Configuration | Outputs | Min. | Max. | Unit |
|---|-----------------|----------------|------|------|------|
| Modulation Frequency | All (except -1) | | 30.0 | 33.0 | kHz |
| Down Spread Margin at the Fundamental Frequency | -11S | CPU, PCI | 0.0 | -0.6 | % |
| Down Spread Margin at the Fundamental Frequency | -21S | CPU, PCI, APIC | 0.0 | -0.6 | % |

Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.

Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

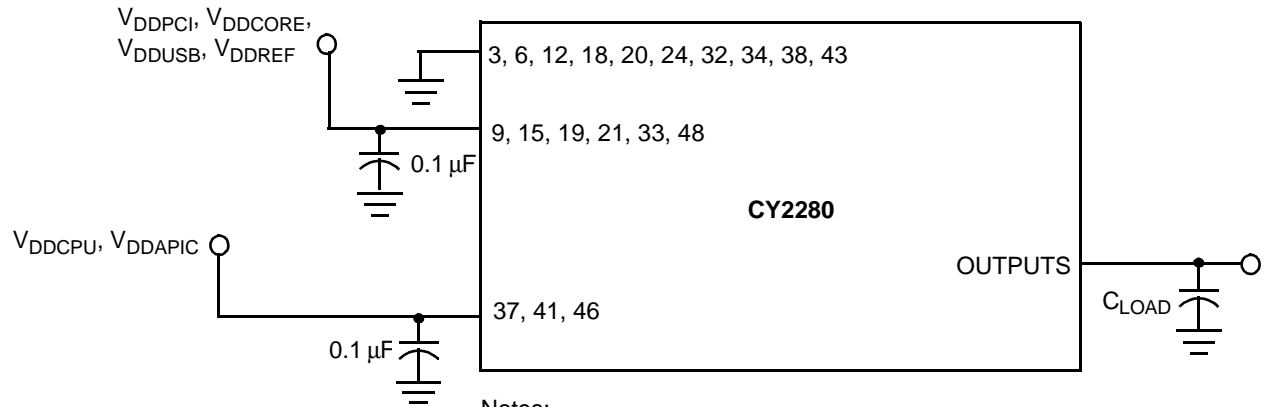
Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

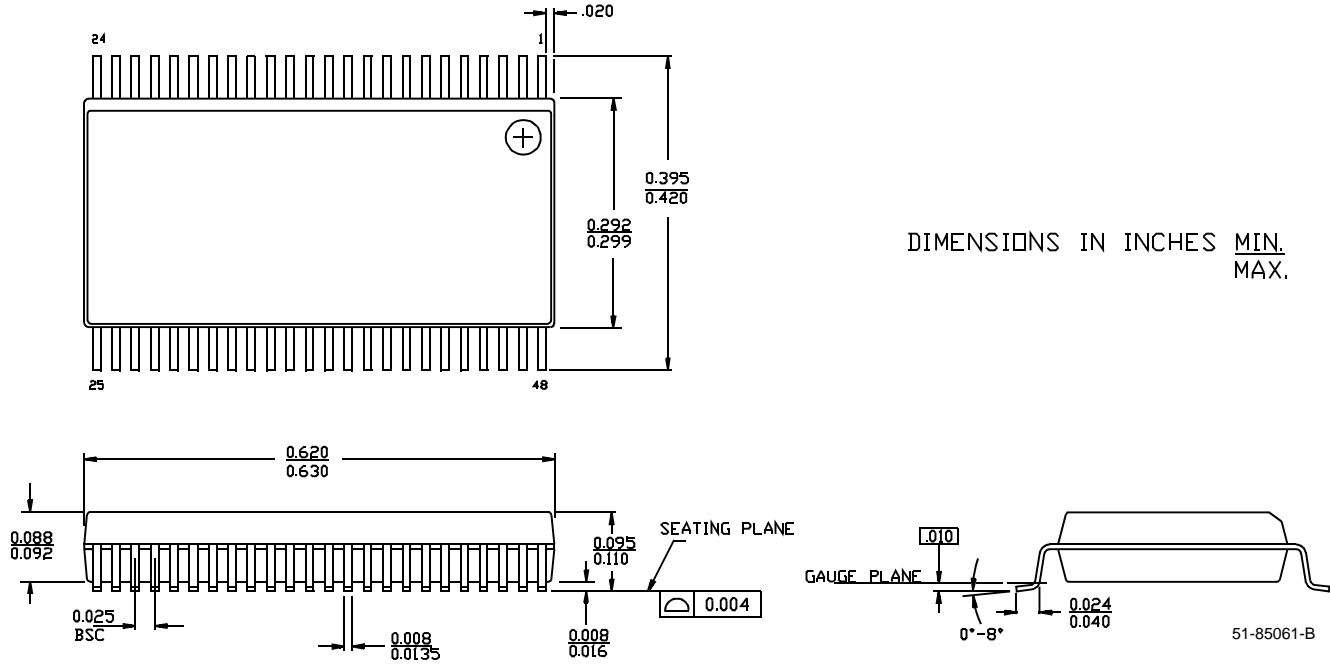
$$R_{series} > R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50 Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 μ F–22 μ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit


Notes:
 Each supply pin must have an individual decoupling capacitor.
 All capacitors must be placed as close to the pins as is possible.

Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---------------|--------------|--------------|-----------------|
| CY2280PVC-1 | O48 | 48-Pin SSOP | Commercial |
| CY2280PVC-11S | O48 | 48-Pin SSOP | Commercial |
| CY2280PVC-21S | O48 | 48-Pin SSOP | Commercial |

Package Diagram
48-Lead Shrunken Small Outline Package O48


Revision History

| Document Title: CY2280 100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum for Mobile or Desktop PCs | | | | |
|---|----------------|-------------------|------------------------|---|
| Document Number: 38-07207 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 111721 | 12/16/01 | DSG | Change from Spec number: 38-00694 to 38-07207 |
| *A | 121842 | 12/14/02 | RBI | Power up requirements added to Operating Conditions Information |