## STW23N85K5



# N-channel 850 V, 0.2 Ω typ., 19 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

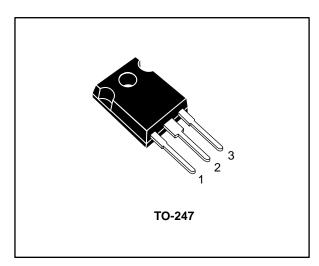
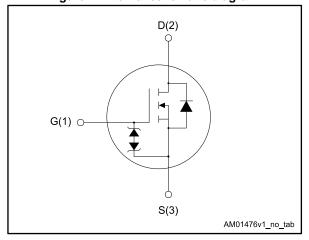


Figure 1: Internal schematic diagram



#### **Features**

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	Ртот
STW23N85K5	850 V	0.275 Ω	19 A	250 W

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

#### **Applications**

• Switching applications

### **Description**

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

**Table 1: Device summary** 

Order code	Marking	Package	Packing
STW23N85K5	23N85K5	TO-247	Tube

Contents STW23N85K5

# Contents

1	Electric	cal ratings	3
2	Electric	cal characteristics	4
	2.1	Electrical characteristics (curves)	6
3	Test cir	·cuits	9
4	Packag	e information	10
	4.1	TO-247 package information	10
5	Revisio	n history	12

STW23N85K5 Electrical ratings

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V <sub>GS</sub>	Gate-source voltage	±30	V	
	Drain current (continuous) at T <sub>case</sub> = 25 °C	19	^	
I <sub>D</sub>	Drain current (continuous) at T <sub>case</sub> = 100 °C	12.4	А	
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	250	А	
P <sub>TOT</sub>	Total dissipation at T <sub>case</sub> = 25 °C	250	W	
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	6	V/ns	
T <sub>stg</sub>	Storage temperature		٥,0	
T <sub>j</sub>	Operating junction temperature	-55 to 150 °C		

#### Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	0.5	۰۵۸۸
R <sub>thj-amb</sub>	Thermal resistance junction-ambient 45		°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub> <sup>(1)</sup>	Avalanche current, repetitive or not repetitive	6	Α
E <sub>AS</sub> <sup>(2)</sup>	Single pulse avalanche energy	200	mJ

#### Notes:

 $<sup>^{\</sup>left( 1\right) }$  Pulse width is limited by safe operating area.

 $<sup>^{(2)}</sup>$   $I_{SD} \leq$  19 A, di/dt=100 A/µs;  $V_{DS}$  peak <  $V_{(BR)DSS},$   $V_{DD}$  = 80%  $V_{(BR)DSS}.$ 

 $<sup>^{(1)}</sup>$  Pulse width limited by  $T_{jmax}$ .

 $<sup>^{(2)}</sup>$  starting  $T_{j}$  = 25 °C,  $I_{D}$  =  $I_{AR},\,V_{DD}$  = 50 V.

Electrical characteristics STW23N85K5

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	850			٧
7	Zoro goto voltago	$V_{GS} = 0 \text{ V}, V_{DS} = 850 \text{ V}$			10	
I <sub>DSS</sub>	I <sub>DSS</sub> Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 850 \text{ V},$ $T_{case} = 125 \text{ °C}$			50	μΑ
I <sub>GSS</sub>	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±10	μΑ
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100 \mu A$	3	4	5	>
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.5 A		0.2	0.275	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		ı	1650	ı	
C <sub>oss</sub>	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$	ı	115	ı	pF
C <sub>rss</sub>	Reverse transfer capacitance	$V_{GS} = 0 V$	ı	2	ı	ρı
Coss eq. (1)	Equivalent output capacitance	$V_{DS} = 0$ to 680 V, $V_{GS} = 0$ V	-	185	-	pF
R <sub>G</sub>	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	1	3.5	ı	Ω
$Q_g$	Total gate charge	$V_{DD} = 520 \text{ V}, I_D = 60 \text{ A},$	ı	38	ı	
$Q_{gs}$	Gate-source charge	V <sub>GS</sub> = 10 V (see <i>Figure 17:</i>	ı	11		nC
$Q_gd$	Gate-drain charge	"Gate charge test circuit")	ı	20	ı	

#### Notes:

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	$V_{DD} = 400 \text{ V}, I_D = 9.5 \text{ A}$	-	22		
t <sub>r</sub>	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$ (see Figure 16: "Switching times	-	14	-	
t <sub>d(off)</sub>	Turn-off delay time	test circuit for resistive load"	-	55	-	ns
t <sub>f</sub>	Fall time	and Figure 21: "Switching time waveform")	-	8	-	

 $<sup>^{(1)}</sup>$   $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		ı		19	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		76	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 19 A	-		1.5	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 19 A, di/dt = 100 A/μs,	1	510		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 60 V (see Figure 18: "Test circuit for inductive load	-	11		μC
I <sub>RRM</sub>	Reverse recovery current	switching and diode recovery times")	-	43		Α
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 19 A, di/dt = 100 A/µs,	-	684		ns
Q <sub>rr</sub>	Reverse recovery charge	$V_{DD}$ = 60 V, $T_j$ = 150 °C (see Figure 18: "Test circuit for	-	14		μC
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times")	-	41		Α

#### Notes:

<sup>&</sup>lt;sup>(1)</sup> Pulse width is limited by safe operating area.

 $<sup>^{(2)}</sup>$  Pulse test: pulse duration = 300  $\mu s,$  duty cycle 1.5%.

# 2.1 Electrical characteristics (curves)

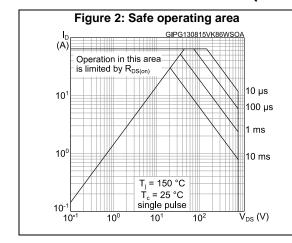
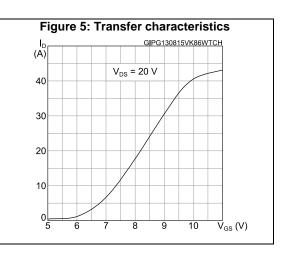
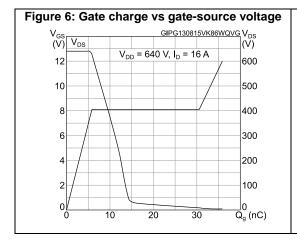
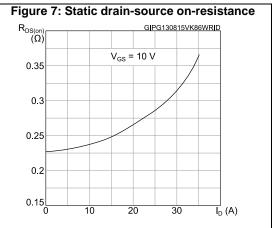


Figure 3: Thermal impedance K
GC20530  $\delta = 0.5$   $\delta = 0.2$   $\delta = 0.1$   $\delta = 0.05$   $\delta = 0.05$   $\delta = 0.01$ Single pulse  $\delta = 0.01$   $\delta = 0.01$   $\delta = 0.01$   $\delta = 0.01$ 

Figure 4: Output characteristics GIPG130815VK86WOCH I<sub>D</sub> (A) 40  $V_{GS} = 10 \text{ V}$  $V_{GS} = 9 V$ 30  $V_{GS} = 8 \text{ V}$ 20  $V_{GS} = 7 V$ 10  $V_{GS} = 6 V$  $V_{GS} = 5 V$ 12 16  $\overrightarrow{V}_{DS}(V)$ 







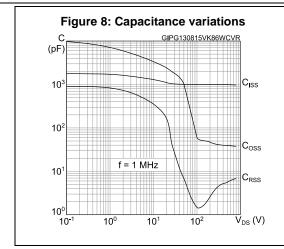
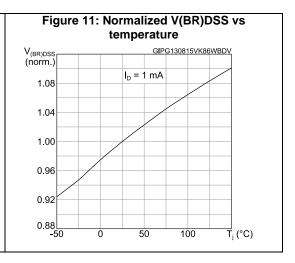
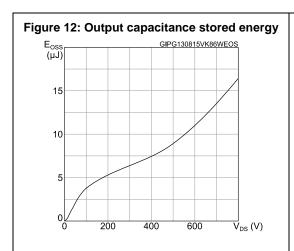


Figure 10: Normalized on-resistance vs temperature

R<sub>DS(on)</sub> GIPG130815VK86WRON
(norm.)
2.6
2.2
1.8
1.4
1.0
0.6
0.2
-50
0
50
100
T<sub>j</sub> (°C)





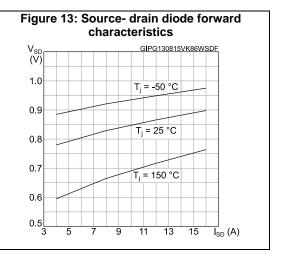
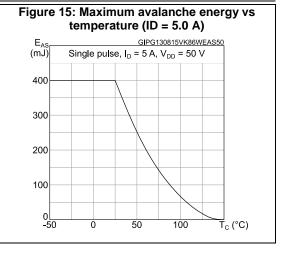


Figure 14: Maximum avalanche energy vs temperature (ID = 3.5 A)

E<sub>AS</sub>
(mJ)
Single pulse, I<sub>D</sub> = 3.5 A, V<sub>DD</sub> = 50 V

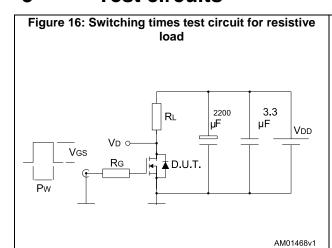
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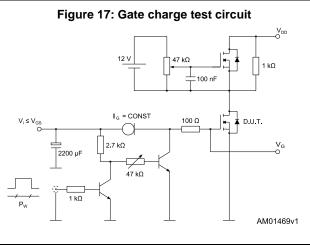
٦, (°C)

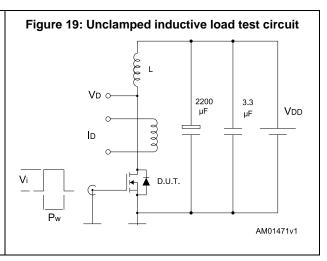


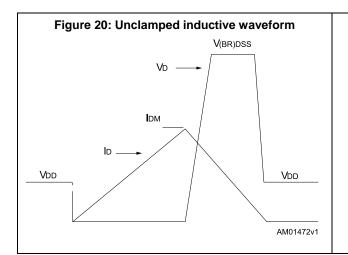
STW23N85K5 Test circuits

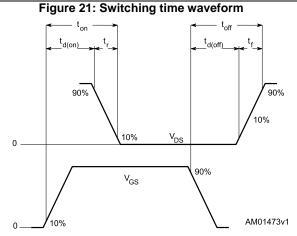
## 3 Test circuits











# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

## 4.1 TO-247 package information

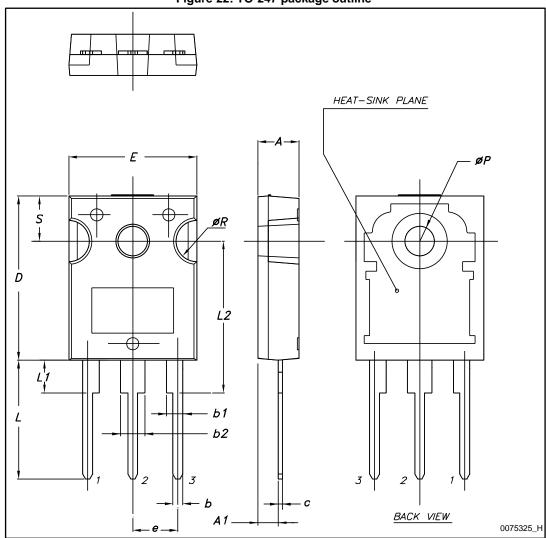


Figure 22: TO-247 package outline

Table 9: TO-247 package mechanical data

Dim		mm.	
Dim.	Min.	Тур.	Max.
А	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
С	0.40		0.80
D	19.85		20.15
E	15.45		15.75
е	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history STW23N85K5

# 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
06-Aug-2012	1	First release.
21-Jan-2014	2	Document status promoted from preliminary to production data.  Added Figure 12: Maximum avalanche energy vs temperature.
13-Aug-2015	3	Text and formatting changes throughout document. On cover page: - updated Title, Features and Description Updated Section Electrical characteristics Updated Section Electrical characteristics (curves) Updated and renamed Section Package information (was Package mechanical data)

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